Enrollment No./Seat No.:

GUJARAT TECHNOLOGICAL UNIVERSITY

Bachelor of Engineering - SEMESTER - III EXAMINATION - WINTER 2025

Subject Code: BE03000181 **Date: 19-12-2025**

Subject Name: Digital System Design

Time: 10:30 AM TO 01:00 PM **Total Marks: 70**

Instructions

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Convert the binary number 101101101 to decimal and hexadecimal.	**03**
	(b)	Simplify F=(A+B)(A+B′)(A′+C) using Boolean algebra.	**04**
	(c)	A Boolean function is given as F(A,B,C)=Σ(1,3,5,7) a) Write the SOP and POS forms. b) Simplify using Boolean algebra. c) Draw the logic circuit.	**07**
Q.2	**(a)**	List down advantages of ROM over combinational logic design.	**03**
	(b)	Implement F = AB + A′C using NOR gates only.	**04**
	(c)	Design a 4-bit Ripple Carry Adder using Full Adders. Explain the working with a neat circuit diagram.	**07**
		OR	
	(c)	Design and explain a 4-bit magnitude comparator using logic gates	**07**
Q.3	**(a)**	Compare :Synchronous and asynchronous circuits	**03**
	(b)	Convert a JK flip-flop into D flip-flop.	**04**
	(c)	Design a circuit to implement a 2-bit binary counter using T flip-flops.	**07**
		OR	
	(a)	Explain state reduction and state assignment in a state machine.	**03**
	(b)	What are race-around conditions in JK flip-flop? How can it be avoided?	**04**
	(c)	Design a 3-bit synchronous up counter using JK flip-flops.	**07**
Q.4	**(a)**	What is the difference between PLA and PAL?	**03**
	(b)	Explain the operation of 4 bit ripple counter with neat circuit and timing diagram a	**04**
	(c)	Explain input forming logic and output forming logic in state machines with example.	**07**
		OR	
	(a)	Explain the working of a 4 x 1 multiplexer with truth table and logic diagram.	**03**

	(b)	Differentiate between Moore and Mealy machines with examples.	**04**
	(c)	Explain the working of a BCD adder in detail with block diagram and necessary logic expressions.	**07**
Q.5	**(a)**	What is resolution of DAC? Name two commonly used DAC ICs.	**03**
	(b)	List the important specifications of ADC and explain any two.	**04**
	(c)	Design an 8-bit R-2R DAC for 5V reference and calculate output for input 10101100.	**07**

OR

	(a)	What is fan-out? Give typical values for TTL and CMOS.	**03**
	(b)	Explain the term “Noise Margin” and how it differs in TTL and CMOS.	**04**
	(c)	Explain TTL NAND gate in detail with internal circuit, working and voltage levels.	**07**

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