Enrolment No./Seat No_____

# GUJARAT TECHNOLOGICAL UNIVERSITY

**BE- SEMESTER–III EXAMINATION – WINTER 2025**

**Subject Code:3131102 Date:15-12-2025**

**Subject Name: Digital System Design**

**Time:10:30 AM TO 01:00 PM Total Marks:70**

**Instructions:**

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

| | | | **Marks** |
|---|---|---|---|
| **Q.1** | **(a)** | Perform following subtraction using 2's complement method. $(11010)_2 - (10000)_2$ | **03** |
| | **(b)** | State & prove De Morgan's theorems with the help of truth tables. | **04** |
| | **(c)** | Simplify the following Boolean expression by means of the Tabulation method. $F(A,B,C,D) = \sum m(0,1,2,4,6,8,9,11,13,15)$ | **07** |
| **Q.2** | **(a)** | Converts the following nos.<br>(i) $(52)_{10} = (\ )_2$<br>(ii) $(436)_8 = (\ )_{16}$<br>(iii) $(5C7)_{16} = ()_{10}$ | **03** |
| | **(b)** | Show that $(A \oplus B \oplus C)' = (A \odot B \odot C)$ | **04** |
| | **(c)** | Express Boolean function in Standard Form also Find the Minterms & Maxterms.<br>(i) $F(A,B,C) = AB + A'C$<br>(ii) $F(A,B,C,D) = A + B$ | **07** |
| | | **OR** | |
| | **(c)** | Design a 4 bit binary to Excess-3 converter. | **07** |
| **Q.3** | **(a)** | What is race around condition in JK flip-flop. | **03** |
| | **(b)** | Design 3-bit odd parity Generator. | **04** |
| | **(c)** | Explain SR Flip-Flop circuit using its symbol, block diagram, truth table and characteristics equation. | **07** |
| | | **OR** | |
| **Q.3** | **(a)** | Draw logic diagram, graphical symbol and Characteristic table for clocked D flip-flop. | **03** |
| | **(b)** | Compare ROM, PLA and PAL. | **04** |
| | **(c)** | Explain Master Slave JK flip-flop with truth table and circuit diagram. | **07** |
| **Q.4** | **(a)** | Discuss general state machine architecture. | **03** |
| | **(b)** | Implement the following expression using 8:1 mux $F(A,B,C,D)=\sum m(0,1,3,5,7,10,11,13,14,15)$. | **04** |
| | **(c)** | Draw and explain Ring counter. | **07** |
| | | **OR** | |
| **Q.4** | **(a)** | Explain edge triggering and level triggering. | **03** |
| | **(b)** | Explain full adder and design a full adder circuit using 3 to 8 decoder and two OR gates. | **04** |
| | **(c)** | Design Modulo-8 counter using T flip-flop. | **07** |

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|---|---|---|---|
| **Q.5** | **(a)** | Give comparison of TTL and CMOS family. | **03** |
| | **(b)** | Explain different modeling styles in Verilog. | **04** |
| | **(c)** | Describe the operation of Bi-directional Shift Register with parallel load With necessary logic diagram. | **07** |

**OR**

| | | | |
|---|---|---|---|
| **Q.5** | **(a)** | Define: i) Power dissipation ii) Noise Margin iii) Figure of merit | **03** |
| | **(b)** | Explain Moore machine. | **04** |
| | **(c)** | Write a short note on FPGA. | **07** |

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