Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER–V EXAMINATION – WINTER 2025

Subject Code:3151105 Date:25-11-2025

Subject Name:VLSI Design

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	What is chip reliability? List the four major causes of chip reliability issues.	**03**
	(b)	Explain the channel length modulation effect in n-channel MOSFET operation.	**04**
	(c)	Explain the MOS system under external bias for accumulation and depletion region.	**07**
Q.2	**(a)**	What is substrate bias effect?	**03**
	(b)	Compare and explain the full custom and semi-custom design style of VLSI.	**04**
	(c)	Draw and explain the basic steps of Local oxidation of Silicon (LOCOS) process.	**07**
		OR	
	(c)	Explain the process steps for fabrication of n-channel MOSFET.	**07**
Q.3	**(a)**	Explain RC delay models for calculation of interconnect delay.	**03**
	(b)	For depletion load n MOS inverter circuit, derive the equation of V_{IL}.	**04**
	(c)	Consider the CMOS inverter circuit with following parameters: V_{DD} = 3.3V, k_n =200 μA/V^2, k_p =80 μA/V^2, $V_{TO,n}$ = 0.6V, $V_{TO,p}$ = -0.7V. Calculate the V_{IL} and V_{OH} on the VTC of the inverter.	**07**
		OR	
Q.3	**(a)**	Draw the circuit of 2 input CMOS NAND gate and explain its working with the help of truth table.	**03**
	(b)	Why in symmetrical and ideal CMOS inverter required (W/L)p ≈ 2.5 (W/L)n ? Explain in detail.	**04**
	(c)	Consider a resistive load inverter circuit with V_{DD}= 5V, k'$_n$ =20μA/V^2, V_{TO} = 0.8V, R_L = 200 kΩ and W/L =2. Calculate V_{OL} and V_{IH} on the VTC of the inverter.	**07**
Q.4	**(a)**	Explain AOI (AND-OR-INVERT) and OAI (OR-AND-INVERT) circuit categories with example for CMOS logic.	**03**
	(b)	Derive switching power dissipation equation of CMOS inverter.	**04**
	(c)	How logic "1" transfer happens in nMOS pass transistor circuits. Explain with suitable example.	**07**
		OR	
Q.4	**(a)**	Draw the AOI based implementation of the clocked NOR based SR latch circuit.	**03**
	(b)	Implement XOR function using CMOS TG (Transmission Gates).	**04**

	(c)	Explain various on chip clock generation circuits and distribution networks.	**07**

Q.5	**(a)**	Draw the CMOS implementation of D-latch.	**03**
	(b)	What is controllability and observability for design for testability (DFT)?	**04**
	(c)	How pre-charge and evaluate logic works for dynamic CMOS circuit? Explain with example.	**07**

OR

Q.5	**(a)**	Compare FinFET and Planner MOSFET.	**03**
	(b)	Explain scan-based techniques for DFT with one example.	**04**
	(c)	Define propagation delay τ_{PHL} and obtain its expression for CMOS inverter circuit.	**07**