Enrollment No./Seat No.:

GUJARAT TECHNOLOGICAL UNIVERSITY

Bachelor of Engineering - SEMESTER - V EXAMINATION - WINTER 2025

Subject Code: 3151107 **Date: 19-11-2025**

Subject Name: Advance Microcontroller

Time: 10:30 AM TO 01:00 PM **Total Marks: 70**

Instructions

1. Attempt all questions.

2. Make suitable assumptions wherever necessary.

3. Figures to the right indicate full marks.

4. Simple and non-programmable scientific calculators are allowed.

			Marks
Q.1	**(a)**	Write three features of the ARM processor family.	**03**
	(b)	What is the RISC design philosophy?	**04**
	(c)	Describe the ARM design philosophy in detail. Explain why ARM became popular in embedded systems.	**07**
Q.2	**(a)**	What is endianness? Differentiate between little-endian and big-endian.	**03**
	(b)	Write a short note on ARM7TDMI interface signals.	**04**
	(c)	Discuss pipeline hazards in ARM processors and explain how data forwarding helps overcome them.	**07**
		OR	
	(c)	Describe the ARM memory map and load-store architecture with an example.	**07**
Q.3	**(a)**	Differentiate between a processor core and a CPU core.	**03**
	(b)	Explain following instructions.1.SWP R0, R1, [R2] 2.MOV R0, R1, LSL R2	**04**
	(c)	Explain ARM program control flow instructions (B, BL, BX) with examples.	**07**
		OR	
	(a)	Explain working of various multiply instructions in ARM with proper example.	**03**
	(b)	Describe following instructions with suitable example. (1) LDMIA R1, {R2-R10} (2) LDMDB R1!, {R2-R10}	**04**
	(c)	Discuss ARM exception handling mechanism with reset example.	**07**
Q.4	**(a)**	Define pointer aliasing in Embedded C. Why is it a concern?	**03**
	(b)	Explain how inline functions differ from normal functions in ARM C. Give an example.	**04**
	(c)	Compare SPI and I2C in terms of protocol, speed, and usage in ARM Embedded C.	**07**
		OR	
	(a)	Describe following assembler directives:ENTRY, ADR, DCD	**03**

	(b)	Why FIQ response is fast than IRQ response in ARM processor? Explain necessity of FIQ with one example.	**04**
	(c)	List optimization techniques of Embedded C Programming. Explain any three techniques in detail with examples.	**07**
Q.5	**(a)**	Explain ARM MPU (Memory Protection Unit) with an example.	**03**
	(b)	Compare unified cache and split cache.	**04**
	(c)	Explain hierarchical memory organization in ARM systems and the role of each level.	**07**

OR

	(a)	Differentiate between paging and segmentation.	**03**
	(b)	Differentiate AHB and APB bus transfers.	**04**
	(c)	Compare Cortex-M, Cortex-R, and Cortex-A in the context of AMBA interconnect usage.	**07**

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