Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER–VI EXAMINATION – WINTER 2025

Subject Code:3161009 Date:25-11-2025

Subject Name:Embedded Systems

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Describe criteria to choose microcontroller for designing embedded system.	**03**
	(b)	Describe use of FPGA and SoC to design Embedded system.	**04**
	(c)	Describe CAN bus protocol with merits and demerits.	**07**
Q.2	**(a)**	Compare Synchronous and Asynchronous serial communication method.	**03**
	(b)	Describe how WDT can used to solve unavoidable software loop.	**04**
	(c)	Compare UART, SPI, I2C, USB protocol for different criteria.	**07**
		OR	
	(c)	Describe AMBA protocol and its variant.	**07**
Q.3	**(a)**	Define Interrupt Deadline. How embedded software designer solve interrupt deadline problem?	**03**
	(b)	Describe use of DMA in embedded system design for data transfer form IO device to memory.	**04**
	(c)	Describe different types of semaphore and its related OS level functions. How it can be used as resource handling mechanism?	**07**
		OR	
Q.3	**(a)**	Define interrupt latency. Describe equations to find interrupt latency.	**03**
	(b)	Describe types of device driver with examples.	**04**
	(c)	Describe priority inversion problem. How to solve it?	**07**
Q.4	**(a)**	Define RTOS. Describe its type with examples.	**03**
	(b)	Describe Function Queue Scheduling mechanism.	**04**
	(c)	Describe Mailbox functions and RPC used for inter-process communication.	**07**
		OR	
Q.4	**(a)**	Compare pre-emptive and co-operative scheduling mechanism.	**03**
	(b)	Describe Earlier Deadline First (EDF) scheduling mechanism.	**04**
	(c)	Describe Lock, Unlock and Spin-lock mechanism used for inter-process communication.	**07**

Q.5 **(a)** Describe MSP430 block diagram and CPU registers. **03**

(b) Describe how to achieve low-power modes in MSP430. **04**

(c) Write a MSP430 C-program to transmit "GTU EXAM" continuously using UART at 9600 baudrate. Assume SMCLK = 1MHz **07**

OR

Q.5 **(a)** Enlist features of ADC10 block in MSP430. For MSP430, Why CPU temperature and power supply is converted in digital? **03**

(b) Describe clocking system in MSP430. Is it possible to drive all peripherals of MSP430 at master clock speed? Justify your answer. **04**

(c) Sketch interfacing diagram to interface one switch at P1.3 and two LEDs at P1.0 and P1.6 with MSP430 board. Write C-program to do following **07**

Switch (P1.3)	LED1 (P1.0)	LED2 (P1.6)
Pressed (Logic-0)	ON	OFF
Released (Logic-1)	OFF	ON

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