Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER–VII EXAMINATION – WINTER 2025

Subject Code:3171111 Date:13-11-2025

Subject Name:Testing and Verification

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

Q.1	**(a)**	Differentiate following terms: Testing and Verification	**03**
	(b)	Calculate number of collapsed faults for two input CMOS NOR Gate.	**04**
	(c)	Explain testing methodology for transistor faults in two-input CMOS NAND Gate.	**07**
Q.2	**(a)**	Write the down levels of abstraction in VLSI Testing.	**03**
	(b)	Obtain Controllability and Observability for various signals of 4 inputs AND using SCOAP and Probability based testability analysis.	**04**
	(c)	Explain Muxed-D full scan design architecture in detail with necessary waveform.	**07**
		OR	
	(c)	What is test point insertion? Explain observation point insertion.	**07**
Q.3	**(a)**	Explain the role of Scan Configuration in Scan design flow.	**03**
	(b)	List down Typical Ad hoc DFT techniques.	**04**
	(c)	List down different types of Scan architectures and explain any one in brief.	**07**
		OR	
Q.3	**(a)**	Draw Concurrent fault simulation flowchart.	**03**
	(b)	What is scan reordering? List and explain different types of it.	**04**
	(c)	Prepare a table showing different design style with Scan design rule and recommended solution.	**07**
Q.4	**(a)**	Explain compile code simulation.	**03**
	(b)	List down different alternative to fault simulation.	**04**
	(c)	Describe parallel fault simulation method with example in detail.	**07**
		OR	
Q.4	**(a)**	What is convergence model in verification?	**03**
	(b)	Write down importance of assertions in verification.	**04**
	(c)	Explain various timing models.	**07**
Q.5	**(a)**	Explain: black box verification and White box verification	**03**
	(b)	Design half subtractor and write it test bench using any hardware description language	**04**
	(c)	List down different types of simulation models and explain any one of them.	**07**
		OR	
Q.5	**(a)**	Discuss limitations of linting tools.	**03**
	(b)	System Verilog is preferred over other hardware verification languages to implement Test Benches in industry. Why?	**04**
	(c)	What is code coverage? List down various types of code coverage. Explain any two in detail	**07**

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