

# GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER-IV EXAMINATION – WINTER 2025

Subject Code:3140707

Date:18-11-2025

Subject Name:Computer Organization & Architecture

Time:02:30 PM TO 05:00 PM

Total Marks:70

Instructions:

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.
4. Simple and non-programmable scientific calculators are allowed.

	MARKS
<b>Q.1</b> (a) Explain following terms in brief. 1. Effective address 2. BSA instruction 3. Micro-operation	<b>03</b>
(b) Explain any two shift micro-operations with examples.	<b>04</b>
(c) What is an assembler? Explain basic computer's assembler with flow charts.	<b>07</b>
<b>Q.2</b> (a) Differentiate RISC and CISC architecture.	<b>03</b>
(b) Explain 5-stage instruction pipeline with example.	<b>04</b>
(c) Describe the control unit of the basic computer with block diagram.	<b>07</b>
<b>OR</b>	
(c) What is an interrupt? Explain interrupt cycle with flowchart.	<b>07</b>
<b>Q.3</b> (a) Write the Flynn's classification of parallel processing and briefly explain any one class.	<b>03</b>
(b) Draw a 4-bit incrementer circuit using full adder.	<b>04</b>
(c) Explain any seven addressing modes with appropriate example.	<b>07</b>
<b>OR</b>	
<b>Q.3</b> (a) List all the major difficulties in pipeline and briefly explain any one	<b>03</b>
(b) Explain address sequencing in the micro programmed control unit	<b>04</b>
(c) Write the importance of the overlapped register window? Compute window size and total number of register for following window organization. Number of window=4, Global register =5, local register in each window= 5 and common register to two window = 3.	<b>07</b>
<b>Q.4</b> (a) Briefly explain the Daisy-Chaining priority.	<b>03</b>
(b) Write short note on the DMA.	<b>04</b>
(c) Explain the booth's algorithm with an appropriate example.	<b>07</b>
<b>OR</b>	
<b>Q.4</b> (a) Explain source-initiated asynchronous data transfer using handshaking.	<b>03</b>
(b) Write short note on the input-output processor.	<b>04</b>
(c) Draw and explain flow chart for the floating point multiplication.	<b>07</b>
<b>Q.5</b> (a) What is the cache coherence? What is the solution to cache coherence problem?	<b>03</b>

- (b) Compare tightly coupled and loosely coupled multiprocessors. **04**  
(c) List various cache mappings. Explain any one in detail. **07**

**OR**

- Q.5** (a) What are the characteristics of multiprocessors? **03**  
(b) Explain the 8 \* 8 omega switching network with diagram. **04**  
(c) Why is the virtual memory? Explain the address mapping in detail. **07**

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