Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER–IV EXAMINATION – WINTER 2025

Subject Code:3140707 Date:18-11-2025

Subject Name:Computer Organization & Architecture

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Explain following terms in brief. 1. Effective address 2. BSA instruction 3. Micro-operation	**03**
	(b)	Explain any two shift micro-operations with examples.	**04**
	(c)	What is an assembler? Explain basic computer's assembler with flow charts.	**07**
Q.2	**(a)**	Differentiate RISC and CISC architecture.	**03**
	(b)	Explain 5-stage instruction pipeline with example.	**04**
	(c)	Describe the control unit of the basic computer with block diagram.	**07**
		OR	
	(c)	What is an interrupt? Explain interrupt cycle with flowchart.	**07**
Q.3	**(a)**	Write the Flynn's classification of parallel processing and briefly explain any one class.	**03**
	(b)	Draw a 4-bit incrementer circuit using full adder.	**04**
	(c)	Explain any seven addressing modes with appropriate example.	**07**
		OR	
Q.3	**(a)**	List all the major difficulties in pipeline and briefly explain any one	**03**
	(b)	Explain address sequencing in the micro programmed control unit	**04**
	(c)	Write the importance of the overlapped register window? Compute window size and total number of register for following window organization. Number of window=4, Global register =5, local register in each window= 5 and common register to two window = 3.	**07**
Q.4	**(a)**	Briefly explain the Daisy-Chaining priority.	**03**
	(b)	Write short note on the DMA.	**04**
	(c)	Explain the booth's algorithm with an appropriate example.	**07**
		OR	
Q.4	**(a)**	Explain source-initiated asynchronous data transfer using handshaking.	**03**
	(b)	Write short note on the input-output processor.	**04**
	(c)	Draw and explain flow chart for the floating point multiplication.	**07**
Q.5	**(a)**	What is the cache coherence? What is the solution to cache coherence problem?	**03**

	(b)	Compare tightly coupled and loosely coupled multiprocessors.	**04**
	(c)	List various cache mappings. Explain any one in detail.	**07**

OR

Q.5	**(a)**	What are the characteristics of multiprocessors?	**03**
	(b)	Explain the 8 * 8 omega switching network with diagram.	**04**
	(c)	Why is the virtual memory? Explain the address mapping in detail.	**07**

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Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER–IV (NEW) EXAMINATION – WINTER 2024

Subject Code:3140707 Date:22-11-2024

Subject Name:Computer Organization & Architecture

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Explain signed representation of integer in computer. Write $(-12)_{10}$ in binary with 8 – bits using following representations (i) Signed magnitude (ii) Signed 1's complement (iii) Signed 2's complement	**03**
	(b)	List all registers used in 'Basic Computer' including their symbolic name, size and functionality.	**04**
	(c)	Explain memory reference instructions of 'Basic Computer'.	**07**
Q.2	**(a)**	Draw block diagram for 4-bit adder – subtractor.	**03**
	(b)	Write an assembly language program to add 50 numbers using a loop.	**04**
	(c)	Explain register stack and memory stack organizations.	**07**
		OR	
	(c)	Write three address and two address instructions program for the following arithmetic expression. Discuss advantages and limitations of both types of programs. X = (A * B / C) + (D / E)	**07**
Q.3	**(a)**	List and explain conflicts that occur in an instruction pipeline.	**03**
	(b)	Briefly explain address sequencing in microprogrammed control unit.	**04**
	(c)	Differentiate RISC and CISC.	**07**
		OR	
Q.3	**(a)**	Write a short note on SIMD array processor.	**03**
	(b)	Explain Fetch subroutine of microprogrammed control.	**04**
	(c)	Explain addition and subtraction with signed magnitude data. Also list hardware required for the same.	**07**
Q.4	**(a)**	Explain any three addressing modes with suitable example.	**03**
	(b)	Differentiate isolated I/O and memory mapped I/O	**04**
	(c)	Explain associative, set-associative and direct mapping of cache memory.	**07**
		OR	
Q.4	**(a)**	Explain functionality of flags used in 'Basic Computer'.	**03**
	(b)	What is handshaking? Explain source initiated data transfer using handshaking with neat diagram.	**04**

	(c)	Write a short note on virtual memory.	**07**
Q.5	**(a)**	Differentiate static RAM and Dynamic RAM.	**03**
	(b)	Write a short note on daisy chain priority interrupt.	**04**
	(c)	Explain any three multiprocessor interconnection structures.	**07**

OR

Q.5	**(a)**	Differentiate tightly coupled and loosely coupled multiprocessor systems.	**03**
	(b)	Write a short note on content addressable memory.	**04**
	(c)	Discuss cache coherence problem and its solutions.	**07**

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Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–IV (NEW) EXAMINATION – WINTER 2023

Subject Code:3140707 Date:19-01-2024

Subject Name: Computer Organization & Architecture

Time: 10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Draw the block diagram of a hypothetical basic computer.	**03**
	(b)	Show different ways to represent fixed-point positive integers including zero.	**04**
	(c)	Explain using flowchart the working of Booth's multiplication algorithm of signed-2's complement numbers.	**07**
Q.2	**(a)**	Which address sequencing capabilities are required in a control memory?	**03**
	(b)	Explain any four Arithmetic operations carried out by ALU.	**04**
	(c)	Discuss various memory hierarchies.	**07**
		OR	
	(c)	Explain the concept of Address Translation and working of the Translation Look-Aside Buffer.	**07**
Q.3	**(a)**	Discuss the importance of "control word" in a processor.	**03**
	(b)	Justify the use of STA instruction in assembly program with an example.	**04**
	(c)	Apply J K flip-flops to design a 3-bit synchronous binary counter.	**07**
		OR	
Q.3	**(a)**	Analyze the 20-bits microinstruction code format with 7 bit used for address.	**03**
	(b)	Apply BUN instruction in assembly program that needs to use a looped sub-routine to check a flag.	**04**
	(c)	Apply the combinational circuits to design a 4-bit adder/subtracter circuit which performs subtraction using 2's complement.	**07**
Q.4	**(a)**	Calculate and show the number of clock cycles required to execute BSA instruction.	**03**
	(b)	Write assembly program for the arithmetic shift-left operation on a number stored in register B. Stop the program in case of overflow.	**04**
	(c)	What is the fundamental difference between a subroutine call and an interrupt request? Analyze the possibility of common memory stack for both.	**07**
		OR	
Q.4	**(a)**	Show the working of LDA instruction using RTL.	**03**
	(b)	Write a program in assembly language to multiply two numbers in registers B and C in case the processor has only ADD instruction.	**04**
	(c)	A subroutine return address can be stored in an index register instead of a stack. Analyze the advantages and disadvantages of both configurations.	**07**
Q.5	**(a)**	A RAM operates with 8-bit data bus, 2 chip select lines and 7-bit address lines. Calculate the number of such RAM chips required to have 512 bytes of main memory.	**03**

	(b)	An address space is specified by 24 bits and the corresponding memory space by 16 bits. How many words are there in the address space and in the memory space?	**04**
	(c)	Discuss various Dynamic Arbitration Algorithms for Interprocessor Arbitration.	**07**

OR

Q.5	**(a)**	Calculate the size of a ROM chip which operates using 8-bit data bus, two chip select lines and 9-bit address bus.	**03**
	(b)	How many 128 x 8 RAM chips are needed to provide a memory capacity of 4096 bytes?	**04**
	(c)	Discuss in brief the interconnection structures of a multiprocessor system.	**07**

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Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–IV(NEW) EXAMINATION – WINTER 2022

Subject Code:3140707 Date:15-12-2022

Subject Name:Computer Organization & Architecture

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Draw the block diagram of 4-bit combinational circuit shifter.	**03**
	(b)	Construct diagram of common bus system of four 4-bits registers with diagram.	**04**
	(c)	What is the role of sequence counter(SC) in control unit? Interpret its concept with the help of its three inputs using diagram.	**07**
Q.2	**(a)**	List out names of eight main registers of basic computer with their symbolic name and purpose.	**03**
	(b)	Summarize following addressing modes with example. 1) Implied mode 2) Register mode	**04**
	(c)	Which are the different phases of Instruction Cycle? Describe Register transfer for fetch phase with its diagram.	**07**
		OR	
	(c)	Define: microinstruction; Identify different types of 16 bits instruction formats for basic computer using figure.	**07**
Q.3	**(a)**	Use BSA and BUN instruction with example and diagram.	**03**
	(b)	Criticize Three-Address Instructions and Zero address instruction with common example.	**04**
	(c)	Describe how control unit determine instruction type after the decoding using flowchart for instruction cycle.	**07**
		OR	
Q.3	**(a)**	Prepare flowchart of CPU-IOP communication.	**03**
	(b)	Differentiate RISC and CISC architecture.	**04**
	(c)	What is cache memory? Interpret direct addressing mapping with diagram.	**07**
Q.4	**(a)**	Draw and criticize memory hierarchy in a computer system.	**03**
	(b)	Write an Assembly level program for addition of 50 numbers.	**04**
	(c)	Draw the flowchart of first pass of the assembler and explain working of the same.	**07**
		OR	
Q.4	**(a)**	Interpret the following instructions: INP, ISZ and LDA	**03**
	(b)	Write an Assembly level program to move one block of data to another location.	**04**
	(c)	List out modes of transfer. Formulate direct memory access technique in detail.	**07**
Q.5	**(a)**	Summarize major hazards in pipelined execution.	**03**

	(b)	What is a data dependency conflict in instruction pipeline? Recommend solutions for data dependency conflicts.	**04**
	(c)	Demonstrate four-segment instruction pipeline in detail	**07**
		OR	
Q.5	**(a)**	Sketch Microinstruction code format. Quote BR and CD field in brief.	**03**
	(b)	Compare following terms: 1. Write through-cache and Write back cache. 2. Spatial locality and Temporal locality	**04**
	(c)	Elaborate flynn's classification scheme with proper diagram.	**07**

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