Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–IV EXAMINATION – SUMMER 2025

Subject Code: 3140707 Date:15-05-2025

Subject Name: Computer Organization & Architecture

Time: 10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Explain the Register Transfer Language with block diagram.	**03**
	(b)	Explain three state bus buffer.	**04**
	(c)	Explain shift micro operations and draw 4-bit combinational circuit shifter.	**07**
Q.2	**(a)**	List and explain any three register reference instruction.	**03**
	(b)	Explain instruction format with its types.	**04**
	(c)	Draw and explain Common Bus System for basic computer register.	**07**
		OR	
	(c)	Explain the basic working principle of the Control Unit with timing diagram.	**07**
Q.3	**(a)**	List out any three register of basic computer.	**03**
	(b)	State various phases of instruction cycle.	**04**
	(c)	Write an assembly level program to find average of 10 numbers stored at consecutive location in memory.	**07**
		OR	
Q.3	**(a)**	Convert following hexadecimal number into decimal, octal and binary. 1) 4A	**03**
	(b)	Explain any 4 addressing modes with example.	**04**
	(c)	What is an Interrupt Cycle? Draw and explain flow chart of it.	**07**
Q.4	**(a)**	Explain register stack.	**03**
	(b)	Write an assembly language program to Add two double precision numbers.	**04**
	(c)	Explain the working of Second Pass Assembler with its flowchart.	**07**
		OR	
Q.4	**(a)**	What is address sequencing?	**03**
	(b)	Write short note on subroutine.	**04**
	(c)	Draw and explain flow chart for multiplication program.	**07**
Q.5	**(a)**	Explain various types of interrupts.	**03**
	(b)	What are status register bits? Draw and explain the block diagram showing all status registers.	**04**
	(c)	Write a note on asynchronous data transfer.	**07**
		OR	
Q.5	**(a)**	What is Memory Interleaving?	**03**
	(b)	Differentiate RISC and CISC.	**04**
	(c)	Explain Flynn's classification for computers.	**07**

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Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–IV (NEW) EXAMINATION – SUMMER 2024

Subject Code:3140707 Date:20-07-2024

Subject Name: Computer Organization & Architecture

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Define RTL. Give an example of register transfer of data through accumulator.	**03**
	(b)	Explain instruction formats with its types.	**04**
	(c)	Explain Instruction cycle with flowchart.	**07**
Q.2	**(a)**	Differentiate MRI and non-MRI.	**03**
	(b)	Explain Memory reference instructions.	**04**
	(c)	Explain micro programmed control organization in detail.	**07**
		OR	
	(c)	What is register stack? Explain push and pop micro-operations.	**07**
Q.3	**(a)**	Explain subroutine call and return with micro-operation.	**03**
	(b)	State the differences between register stack and memory stack.	**04**
	(c)	What is addressing modes? List and explain any five addressing modes by taking proper example(s).	**07**
		OR	
Q.3	**(a)**	Write a short note on memory interleaving.	**03**
	(b)	Explain Flynn's classification of computer.	**04**
	(c)	Explain pipelining technique. Draw the general structure of four segment pipeline.	**07**
Q.4	**(a)**	Explain the role of associative memory.	**03**
	(b)	Explain in brief about Cache memory and Virtual memory.	**04**
	(c)	Discuss associative mapping and direct mapping in organization of cache memory.	**07**
		OR	
Q.4	**(a)**	Explain Content Addressable Memory.	**03**
	(b)	Compare SRAM and DRAM.	**04**
	(c)	Explain paging and address translation with example.	**07**
Q.5	**(a)**	Compare tightly coupled and loosely coupled systems.	**03**
	(b)	Write a note on crossbar switch interconnection structure with block diagram	**04**
	(c)	Describe cache coherence problem and its solutions in detail.	**07**
		OR	
Q.5	**(a)**	Explain CLA, ISZ and CMA instruction.	**03**
	(b)	Draw and explain in brief flowchart for interrupt cycle.	**04**
	(c)	Explain first pass of an assembler with flowchart.	**07**

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Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER– IV(NEW) EXAMINATION – SUMMER 2023

Subject Code:3140707 Date:13-07-2023

Subject Name:Computer Organization & Architecture

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Write the name of basic computer registers with their functionalities.	**03**
	(b)	Discuss 4-bit binary adder with neat diagram.	**04**
	(c)	Enlist various kinds of addressing modes. Explain any five of same and support your answer by taking small example.	**07**
Q.2	**(a)**	Write sequence of microoperations to execute the following instructions: - AND - STA	**03**
	(b)	Write assembly language program to subtract two numbers.	**04**
	(c)	Write two address, one address and zero address instructions program for the following arithmetic expression: X = (A + B) * (C – D / E) + F * G	**07**
		OR	
	(c)	Assume A = + 6 and B = + 7, apply Booth algorithm for multiplying A and B. Make necessary assumptions if required.	**07**
Q.3	**(a)**	Explain Flynn's classification for computers in brief.	**03**
	(b)	Draw the flowchart for first pass of assembler and explain the same in brief.	**04**
	(c)	Elaborate CPU-IOP communication.	**07**
		OR	
Q.3	**(a)**	Explain pipeline conflicts in brief.	**03**
	(b)	Discuss three state bus buffers with neat diagram.	**04**
	(c)	Write a detailed note on associative memory.	**07**
Q.4	**(a)**	Explain DMA in brief.	**03**
	(b)	Write a note on SIMD array processor.	**04**
	(c)	A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part. 1. How many bits are there in operation code, the register code part and the address part? 2. Draw the instruction word format and indicate the number of bits in each part. 3. How many bits are there in the data and address inputs of the memory?	**07**
		OR	
Q.4	**(a)**	Write a brief note on memory hierarchy.	**03**
	(b)	In certain scientific computations it is necessary to perform the arithmetic	**04**

operation (A_i + B_i) * (C_i + D_i) with a stream of numbers. Specify pipeline configuration to carry out this task. List the contents of all registers in the pipeline for i=1 through 4.

(c) Discuss microprogrammed control organization with neat diagram. **07**

Q.5 **(a)** Perform A – B (subtract) operation for the following numbers using signed magnitude number format. (Write necessary assumptions if required) **03**

A = + 11 and B = - 6

(b) Explain status bit conditions with neat diagram. **04**

(c) Discuss cache coherence problem in detail. **07**

OR

Q.5 **(a)** Write the difference(s) between arithmetic shift left and logical shift left instruction. Support your answer with proper illustration. **03**

(b) State the differences between RISC and CISC. **04**

(c) Explain any two types of mapping procedures when considering the organization of cache memory. **07**

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Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–IV (NEW) EXAMINATION – SUMMER 2022

Subject Code:3140707 Date:29-06-2022

Subject Name:Computer Organization & Architecture

Time:10:30 AM TO 01:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	What is binary and decimal equivalent of F8 hexadecimal value?	**03**
	(b)	Write Steps for two n digit numbers subtraction in base r.	**04**
	(c)	List and explain Memory reference instructions in detail.	**07**
Q.2	**(a)**	What is arithmetic micro operation?	**03**
	(b)	What is RAM and ROM?	**04**
	(c)	Draw and explain working of 4 bit binary adder.	**07**
		OR	
	(c)	State and Explain any seven logic micro operation.	**07**
Q.3	**(a)**	List out Register for basic computer.	**03**
	(b)	Explain register reference instruction format.	**04**
	(c)	Explain register transfer using block diagram and timing diagram.	**07**
		OR	
Q.3	**(a)**	Draw and explain control unit diagram for basic computer.	**03**
	(b)	State various phases of instruction cycle.	**04**
	(c)	Explain any four input output reference instruction.	**07**
Q.4	**(a)**	Draw flowchart of first pass assembler.	**03**
	(b)	Write assembly language program to add two numbers.	**04**
	(c)	Write assembly language program to multiply two numbers.	**07**
		OR	
Q.4	**(a)**	What is address sequencing?	**03**
	(b)	Write assembly language program to subtract one number from other number.	**04**
	(c)	Explain booth's multiplication algorithm with example.	**07**
Q.5	**(a)**	Explain register stack.	**03**
	(b)	What is difference between two address and three address instructions?	**04**
	(c)	Write a note on asynchronous data transfer.	**07**
		OR	
Q.5	**(a)**	What is difference between direct and indirect addressing mode?	**03**
	(b)	Explain arithmetic pipeline.	**04**
	(c)	Write a short note on virtual memory.	**07**

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