GUJARAT TECHNOLOGICAL UNIVERSITY

BE-4 SEMESTER – OLD PAPER – S22 TO W25 – QUESTION BANK

Subject Name & Code:
Computer Organization & Architecture (3140707)

Unit 1: Computer Data Representation & Register Transfer

(Total Hrs: 4)

Repeated Questions:

1. **Explain Register Transfer Language with a block diagram.**
   - **Appeared in:** S25 (Q1a, 03 marks)
2. **Explain shift micro-operations and draw a 4-bit combinational circuit shifter.**
   - **Appeared in:** S25 (Q1c, 07 marks), W22 (Q1a, 03 marks)
3. **Explain three-state bus buffer.**
   - **Appeared in:** S25 (Q1b, 04 marks), S23 (Q3b, 04 marks)
4. **What is micro-operation? Explain with an example.**
   - **Appeared in:** W25 (Q1a, 03 marks)
5. **Explain signed representation of integers. Write $(-12)_{10}$ in 8-bit using signed magnitude, 1's complement, and 2's complement.**
   - **Appeared in:** W24 (Q1a, 03 marks)
6. **Draw a 4-bit binary adder with a neat diagram.**
   - **Appeared in:** S23 (Q1b, 04 marks), S22 (Q2c, 07 marks)
7. **Explain arithmetic and logic shift operations with examples.**
   - **Appeared in:** W25 (Q1b, 04 marks)

Other Important Questions:

1. **Define RTL. Give an example of register transfer of data through accumulator.**
   - **Appeared in:** S24 (Q1a, 03 marks)
2. **Explain fixed-point representation of positive integers including zero.**
   - **Appeared in:** W23 (Q1b, 04 marks)
3. **Perform A – B using signed magnitude representation (A = +11, B = -6).**
   - **Appeared in:** S23 (Q5a, 03 marks)
4. **Explain the difference between arithmetic shift left and logical shift left.**
   - **Appeared in:** S23 (Q5a, 03 marks)
5. **Explain the role of the Arithmetic Logic Shift Unit (ALSU).**
   - **Appeared in:** Syllabus Topic
6. **Draw a 4-bit adder-subtractor circuit.**
   - **Appeared in:** W24 (Q2a, 03 marks)
7. **Explain micro-operations for push and pop in a register stack.**
   - **Appeared in:** S24 (Q3a, 03 marks)
8. **Explain the concept of complements in number representation.**
   - **Appeared in:** Syllabus Topic

Unit 2: Basic Computer Organization and Design

(Total Hrs: 4)

Repeated Questions:

1. **List and explain the basic computer registers with their size and functionality.**
   - **Appeared in:** S23 (Q1a, 03 marks), W24 (Q1b, 04 marks), W22 (Q2a, 03 marks)
2. **Explain the instruction cycle with a flowchart.**
   - **Appeared in:** S24 (Q1c, 07 marks), S22 (Q5b, 04 marks)
3. **Explain memory reference instructions in detail.**
   - **Appeared in:** S24 (Q2b, 04 marks), S22 (Q1c, 07 marks), W24 (Q1c, 07 marks)
4. **Differentiate between MRI and non-MRI instructions.**
   - **Appeared in:** S24 (Q2a, 03 marks)
5. **Draw and explain the common bus system for basic computer registers.**
   - **Appeared in:** S25 (Q2c, 07 marks), W22 (Q1b, 04 marks)
6. **Explain the working of the control unit with a timing diagram.**
   - **Appeared in:** S25 (Q2c, 07 marks), S22 (Q5a, 07 marks)
7. **What is address sequencing? Explain.**
   - **Appeared in:** S22 (Q7a, 03 marks), W25 (Q3b, 04 marks)

Other Important Questions:

1. **Explain the role of the Sequence Counter (SC) in the control unit.**
   - **Appeared in:** W22 (Q1c, 07 marks)
2. **Explain the fetch phase of the instruction cycle with register transfers.**
   - **Appeared in:** W22 (Q2c, 07 marks)
3. **Draw the block diagram of a hypothetical basic computer.**
   - **Appeared in:** W23 (Q1a, 03 marks)
4. **Explain the LDA instruction using RTL.**
   - **Appeared in:** W23 (Q4a, 03 marks)
5. **Explain the BSA and BUN instructions with examples.**
   - **Appeared in:** W22 (Q3a, 03 marks)
6. **Write micro-operations for AND and STA instructions.**
   - **Appeared in:** S23 (Q2a, 03 marks)
7. **Explain the complete computer description and design of the accumulator unit.**
   - **Appeared in:** Syllabus Topic
8. **Explain timing and control signals in basic computer design.**
   - **Appeared in:** Syllabus Topic

Unit 3: Assembly Language Programming

(Total Hrs: 8)

Repeated Questions:

1. **Write an assembly language program to add two numbers.**
   - **Appeared in:** S22 (Q6b, 04 marks)
2. **Write an assembly language program to subtract two numbers.**
   - **Appeared in:** S23 (Q2b, 04 marks), S22 (Q7b, 04 marks)
3. **Write an assembly program to find the average of 10 numbers stored in consecutive memory locations.**
   - **Appeared in:** S25 (Q3c, 07 marks)
4. **Write an assembly program to add 50 numbers using a loop.**
   - **Appeared in:** W24 (Q2b, 04 marks), W22 (Q4b, 04 marks)
5. **Explain subroutine call and return with micro-operations.**
   - **Appeared in:** S24 (Q3b, 04 marks)
6. **Write a program using three-address, two-address, and zero-address instructions for:**
   $$X = (A + B) * (C - D/E) + F * G$$
   - **Appeared in:** S23 (Q2c, 07 marks)
7. **Write a program using three-address and two-address instructions for:**
   $$X = (A * B/C) + (D/E)$$
   - **Appeared in:** W24 (Q2c, 07 marks)

Other Important Questions:

1. **Write an assembly program to multiply two numbers.**
   - **Appeared in:** S22 (Q6c, 04 marks)
2. **Write an assembly program to move a block of data to another location.**
   - **Appeared in:** W22 (Q4b, 04 marks)
3. **Explain I/O programming in assembly language.**
   - **Appeared in:** Syllabus Topic
4. **Explain looping constructs in assembly language.**
   - **Appeared in:** Syllabus Topic
5. **Write an assembly program for arithmetic shift-left operation and stop on overflow.**
   - **Appeared in:** W23 (Q4b, 04 marks)
6. **Explain the use of STA instruction with an example.**
   - **Appeared in:** W23 (Q3b, 04 marks)
7. **Explain the BUN instruction in a looped subroutine to check a flag.**
   - **Appeared in:** W23 (Q3b, 04 marks)
8. **Write a program to multiply two numbers using only ADD instruction.**
   - **Appeared in:** W23 (Q4b, 04 marks)

Unit 4: Microprogrammed Control Organization

(Total Hrs: 4)

Repeated Questions:

1. **Explain microprogrammed control organization with a neat diagram.**
    - **Appeared in:** S24 (Q2c, 07 marks), S23 (Q4c, 07 marks)
2. **Explain address sequencing in a microprogrammed control unit.**
    - **Appeared in:** W25 (Q3b, 04 marks), W24 (Q3b, 04 marks)
3. **What is control memory? Explain its importance.**
    - **Appeared in:** Syllabus Topic
4. **Explain the concept of a control word in a processor.**
    - **Appeared in:** W23 (Q3a, 03 marks)

Other Important Questions:

1. **Analyze a 20-bit microinstruction format with a 7-bit address field.**
    - **Appeared in:** W23 (Q3a, 03 marks)
2. **Explain the fetch subroutine in microprogrammed control.**
    - **Appeared in:** W24 (Q3b, 04 marks)
3. **Sketch the microinstruction code format and explain BR and CD fields.**
    - **Appeared in:** W22 (Q5a, 03 marks)
4. **Explain the design of the control unit in microprogramming.**
    - **Appeared in:** Syllabus Topic
5. **Explain microprogram example and sequencing.**
    - **Appeared in:** Syllabus Topic

Unit 5: Central Processing Unit (CPU)

(Total Hrs: 5)

Repeated Questions:

1. **Differentiate between RISC and CISC architectures.**
   - **Appeared in:** S25 (Q5b, 04 marks), W25 (Q2a, 03 marks), W24 (Q3c, 07 marks), W22 (Q3b, 04 marks), S23 (Q5b, 04 marks)
2. **Explain addressing modes with examples.**
   - **Appeared in:** S25 (Q3b, 04 marks), S23 (Q1c, 07 marks), W24 (Q4a, 03 marks), W22 (Q2b, 04 marks)
3. **Explain register stack and memory stack organizations.**
   - **Appeared in:** S25 (Q4a, 03 marks), S24 (Q3a, 03 marks), W24 (Q2c, 07 marks)
4. **Explain general register organization and stack organization.**
   - **Appeared in:** Syllabus Topic
5. **Explain instruction formats and their types.**
   - **Appeared in:** S25 (Q2b, 04 marks), S24 (Q1b, 04 marks)

Other Important Questions:

1. **Explain the difference between two-address and three-address instructions.**
   - **Appeared in:** S22 (Q8b, 04 marks)
2. **Explain implied and register addressing modes with examples.**
   - **Appeared in:** W22 (Q2b, 04 marks)
3. **Criticize three-address and zero-address instructions with a common example.**
   - **Appeared in:** W22 (Q3b, 04 marks)
4. **Explain data transfer and manipulation instructions.**
   - **Appeared in:** Syllabus Topic
5. **Explain program control instructions.**
   - **Appeared in:** Syllabus Topic
6. **Explain the importance of overlapped register windows and calculate window size.**
   - **Appeared in:** W25 (Q3c, 07 marks)
7. **Explain subroutine and its implementation.**
   - **Appeared in:** S25 (Q4b, 04 marks)

Unit 6: Pipeline and Vector Processing

(Total Hrs: 5)

Repeated Questions:

1. **Explain Flynn's classification of computers.**
   - **Appeared in:** S25 (Q5c, 07 marks), S24 (Q3b, 04 marks), S23 (Q3a, 03 marks), W25 (Q3a, 03 marks), W22 (Q5c, 07 marks)
2. **Explain pipeline conflicts/hazards.**
   - **Appeared in:** S23 (Q3a, 03 marks), W24 (Q3a, 03 marks), W25 (Q3a, 03 marks)
3. **Explain pipelining technique and draw a four-segment pipeline.**
   - **Appeared in:** S24 (Q3c, 07 marks), W22 (Q5c, 07 marks)
4. **Explain arithmetic and instruction pipelines.**
   - **Appeared in:** S22 (Q9b, 04 marks), Syllabus Topic
5. **Explain vector processing and array processors.**
   - **Appeared in:** W24 (Q3a, 03 marks), Syllabus Topic

Other Important Questions:

1. **Explain a 5-stage instruction pipeline with an example.**
   - **Appeared in:** W25 (Q2b, 04 marks)
2. **Specify a pipeline configuration for (Ai + Bi) * (Ci + Di) for i=1 to 4.**
   - **Appeared in:** S23 (Q4b, 04 marks)
3. **Explain data dependency conflicts in pipelines and their solutions.**
   - **Appeared in:** W22 (Q5b, 04 marks)
4. **Explain RISC pipeline.**
   - **Appeared in:** Syllabus Topic
5. **Explain parallel processing concepts.**
   - **Appeared in:** Syllabus Topic

Unit 7: Computer Arithmetic

(Total Hrs: 4)

Repeated Questions:

1. **Explain Booth's multiplication algorithm with an example.**
   - **Appeared in:** S23 (Q2c, 07 marks), S22 (Q7c, 07 marks), W23 (Q1c, 07 marks), W25 (Q4c, 07 marks)
2. **Explain addition and subtraction with signed magnitude data.**
   - **Appeared in:** W24 (Q3c, 07 marks)
3. **Explain floating-point arithmetic operations.**
   - **Appeared in:** Syllabus Topic
4. **Explain multiplication and division algorithms.**
   - **Appeared in:** Syllabus Topic

Other Important Questions:

1. **Apply Booth's algorithm to multiply A = +6 and B = +7.**
   - **Appeared in:** S23 (Q2c, 07 marks)
2. **Draw a flowchart for floating-point multiplication.**
   - **Appeared in:** W25 (Q4c, 07 marks)
3. **Explain decimal arithmetic unit.**
   - **Appeared in:** Syllabus Topic
4. **Explain the steps for subtraction of two n-digit numbers in base r.**
   - **Appeared in:** S22 (Q1b, 04 marks)
5. **Explain arithmetic micro-operations.**
   - **Appeared in:** S22 (Q2a, 03 marks)

Unit 8: Input-Output Organization

(Total Hrs: 4)

Repeated Questions:

1. **Explain asynchronous data transfer.**
   - **Appeared in:** S25 (Q5c, 07 marks), S22 (Q8c, 07 marks)
2. **Explain DMA (Direct Memory Access).**
   - **Appeared in:** S23 (Q4a, 03 marks), W25 (Q4b, 04 marks)
3. **Explain interrupt cycle with a flowchart.**
   - **Appeared in:** S25 (Q3c, 07 marks), W25 (Q2c, 07 marks), W24 (Q5b, 04 marks)
4. **Explain priority interrupt (daisy chain).**
   - **Appeared in:** W25 (Q4a, 03 marks), W24 (Q5b, 04 marks)
5. **Explain I/O processor (IOP) and CPU-IOP communication.**
   - **Appeared in:** S23 (Q3c, 07 marks), W22 (Q3a, 03 marks)

Other Important Questions:

1. **Differentiate between isolated I/O and memory-mapped I/O.**
   - **Appeared in:** W24 (Q4b, 04 marks)
2. **Explain handshaking in source-initiated asynchronous data transfer.**
   - **Appeared in:** W25 (Q4a, 03 marks), W24 (Q4b, 04 marks)
3. **Explain modes of data transfer.**
   - **Appeared in:** W22 (Q4c, 07 marks)
4. **Explain serial communication.**
   - **Appeared in:** Syllabus Topic
5. **Explain input-output interface.**
   - **Appeared in:** Syllabus Topic
6. **Explain any four input-output reference instructions.**
   - **Appeared in:** S22 (Q5c, 07 marks)

Unit 9: Memory Organization

(Total Hrs: 6)

Repeated Questions:

1. **Explain cache memory mapping techniques (associative, direct, set-associative).**
   - **Appeared in:** W24 (Q4c, 07 marks), S25 (Q5c, 07 marks), S23 (Q5c, 07 marks), S24 (Q4c, 07 marks)
2. **Explain virtual memory.**
   - **Appeared in:** S22 (Q9c, 04 marks), W24 (Q4c, 07 marks), W25 (Q5c, 07 marks)
3. **Explain memory hierarchy.**
   - **Appeared in:** S23 (Q4a, 03 marks), W22 (Q4a, 03 marks), W23 (Q2c, 07 marks)
4. **Compare SRAM and DRAM / Static RAM vs. Dynamic RAM.**
   - **Appeared in:** S24 (Q4b, 04 marks), W24 (Q5a, 03 marks)
5. **Explain associative memory / content-addressable memory.**
   - **Appeared in:** S24 (Q4a, 03 marks), S23 (Q3c, 07 marks), W24 (Q5b, 04 marks)

Other Important Questions:

1. **Explain paging and address translation with an example.**
   - **Appeared in:** S24 (Q4c, 07 marks), W23 (Q2c, 07 marks)
2. **Explain cache coherence problem and its solutions.**
   - **Appeared in:** S24 (Q5c, 07 marks), S23 (Q5c, 07 marks), W24 (Q5c, 07 marks), W25 (Q5a, 03 marks)
3. **Explain main memory and auxiliary memory.**
   - **Appeared in:** Syllabus Topic
4. **Numerical: Calculate memory size, chips required, address space, etc.**
   - **Appeared in:** W23 (Q5a,b, 03+04 marks), W23 (Q5a,b, 03+04 marks)
5. **Explain the role of TLB (Translation Lookaside Buffer).**
   - **Appeared in:** W23 (Q2c, 07 marks)
6. **Compare write-through and write-back cache.**
   - **Appeared in:** W22 (Q5b, 04 marks)
7. **Explain spatial and temporal locality.**
   - **Appeared in:** W22 (Q5b, 04 marks)

Unit 10: Multiprocessors

(Total Hrs: 4)

Repeated Questions:

1. **Explain multiprocessor interconnection structures.**
    - **Appeared in:** W24 (Q5c, 07 marks), W22 (Q5c, 07 marks), W23 (Q5c, 07 marks)
2. **Compare tightly coupled and loosely coupled multiprocessor systems.**
    - **Appeared in:** S24 (Q5a, 03 marks), W24 (Q5a, 03 marks), W25 (Q5b, 04 marks)
3. **Explain cache coherence in multiprocessors.**
    - **Appeared in:** S24 (Q5c, 07 marks), W25 (Q5a, 03 marks)
4. **Explain interprocessor arbitration and communication.**
    - **Appeared in:** W23 (Q5c, 07 marks), Syllabus Topic

Other Important Questions:

1. **Explain characteristics of multiprocessors.**
    - **Appeared in:** W25 (Q5a, 03 marks)
2. **Explain shared memory multiprocessors.**
    - **Appeared in:** Syllabus Topic
3. **Explain the Omega switching network (8x8) with a diagram.**
    - **Appeared in:** W25 (Q5b, 04 marks)
4. **Explain crossbar switch interconnection with a block diagram.**
    - **Appeared in:** S24 (Q5b, 04 marks)
5. **Explain dynamic arbitration algorithms for interprocessor arbitration.**
    - **Appeared in:** W23 (Q5c, 07 marks)

****