GUJARAT TECHNOLOGICAL UNIVERSITY

BE-4 SEMESTER – OLD PAPER – S22 TO W25 – QUESTION BANK ANSWER

Subject Name & Code:

POWER ELECTRONICS (3140915)

UNIT 1– Power Switching Devices

🔁 REPEATED QUESTIONS

R1. Draw and explain static characteristics of SCR. (4 marks)

Appeared in: S25(3), W25(4), W24(4), W23(4), S23(4) → Highest: 4 marks

Ans:

Static V-I characteristics of SCR show anode current (I_a) vs anode-cathode voltage (V_{ak}) for different gate currents.

- **Forward blocking mode** (off-state): SCR blocks forward voltage with small leakage current (I_{leak}).
- **Forward conduction mode** (on-state): After **breakover voltage (V_{6o})** or gate pulse, SCR latches on; voltage drops to ~1-2V (holding voltage).
- **Reverse blocking mode**: SCR blocks reverse voltage like a diode until reverse breakdown.
- **Latching current (I_l)** & **Holding current (I_h)** marked on curve.

[DG PROMPT]

Title: Static V-I Characteristics of SCR

Description: Draw two quadrants (forward and reverse). X-axis: V_{ak} (Volts), Y-axis: I_a (mA/A). In forward quadrant: draw curve starting from origin, small leakage current plateau, then sudden rise at V_{6o}, then vertical drop to low voltage (on-state). Show multiple curves for increasing I_G ($I_G1 < I_G2 < I_G3$). Mark latching current (I_l) and holding current (I_h) on on-state portion. In reverse quadrant: draw reverse leakage current with sharp reverse breakdown knee.

Real-world application: Used to design snubber circuits and gate drives in AC-DC converters, motor controllers.

R2. Explain construction, VI characteristics of SCR. (4 marks)

Appeared in: S23(4)

Ans:

- **Construction**: Four-layer PNPN structure (P_1-N_1-P_2-N_2) with three junctions J_1, J_2, J_3. Anode at P_1, Cathode at N_2, Gate at P_2.
- **VI characteristics** (same as R1 above):
  - *Forward blocking*: J_2 reverse biased.
  - *Forward conduction*: Gate trigger reduces breakover voltage.
  - *Reverse blocking*: J_1 and J_3 reverse biased.

Key terms: Latching current – minimum anode current to maintain conduction after gate signal removed.

Holding current – minimum anode current to keep SCR on without gate signal.

R3. Draw the symbol of Transistor, SCR, MOSFET, IGBT, DIAC, TRIAC, GTO. (4 marks)
Appeared in: S24(4), S23(3), W25(3)
Ans:
[DG PROMPT]
Title: Symbols of Power Semiconductor Devices
Description: Draw 7 separate symbols aligned horizontally or in 2 rows.

1. **Transistor (BJT)** – NPN: arrow on emitter pointing outward; PNP: arrow pointing inward.
2. **SCR** – Diode symbol with gate line attached to cathode side at 45°.
3. **MOSFET** – Three terminals: Drain (D), Source (S), Gate (G). Vertical line with gap, gate isolated. Arrow from source to body (for N-channel).
4. **IGBT** – Combination: collector (C) and emitter (E) like BJT, gate (G) like MOSFET.
5. **DIAC** – Two terminals, bidirectional – two parallel diodes facing opposite directions.
6. **TRIAC** – Three terminals (MT1, MT2, Gate) – two SCRs in antiparallel on same symbol.
7. **GTO** – Similar to SCR but with double arrow on gate to indicate turn-off capability.

(Actual drawing to be sketched as per above description)

R4. Explain basic structure of IGBT/MOSFET with schematic diagram. (3 marks)
Appeared in: S25(3)-IGBT, S25(3)-MOSFET, S24(3)-Both
Ans:
MOSFET (Power MOSFET – vertical structure):

- N^+ source, P-body, N^- drift layer, N^+ drain.
- Gate oxide isolated – voltage control.

IGBT:

- P^+ substrate (collector), N^- buffer, P-body, N^+ source (emitter).
- Combines MOSFET gate control with BJT conductivity modulation.

[DG PROMPT]
Title: Basic Structure of Power MOSFET and IGBT
Description: Draw two cross-sections side by side.

- **MOSFET**: Top to bottom: Source metal (N^+) → P-body → N^- epitaxial layer → N^+ substrate → Drain metal. Gate electrode on top with oxide layer over P-body.
- **IGBT**: Top: Emitter metal (N^+) → P-body → N^- drift → N^+ buffer → P^+ collector → Collector metal. Gate similar to MOSFET. Label all layers and terminals (Source/Emitter, Gate, Drain/Collector).

R5. Discuss two transistor model of SCR/Thyristor. (4 marks)
Appeared in: S25(4), S23(3)
Ans:
SCR is represented as two complementary BJTs: **NPN (Q_1)** and **PNP (Q_2)** connected in regenerative feedback.

- **Q_1 (NPN)** – Base = P_2 (gate), Collector = N_2 (cathode), Emitter = N_1? Wait, correct:
  - PNP (Q_2): P_1 (anode) – N_1 – P_2 (base of Q_2) – collector of Q_1? Standard model:
    - Q_1 (NPN): Emitter = N_2 (cathode), Base = P_2, Collector = N_1.
    - Q_2 (PNP): Emitter = P_1 (anode), Base = N_1, Collector = P_2 (gate).
- **Base of Q_1** connected to **collector of Q_2**; **Base of Q_2** connected to **collector of Q_1** → positive feedback.
- When $\alpha_1 + \alpha_2 \rightarrow 1$, SCR latches on.

- Gate current injects base current into Q_1, triggering turn-on.

Real-world application: Explains latching action and temperature sensitivity of SCR.

📌 OTHER IMPORTANT QUESTIONS

O1. Draw only basic structure of power MOSFET and IGBT and name each layer and part. (3 marks)

Appeared in: S24(3), W22(3)

Ans: Same as R4 answer (3-mark version – concise).

[DG PROMPT] Same as R4 but without explanation text. Provide labeled cross-section only.

O2. Explain three different modes of operation of a thyristor with the help of its static V-I characteristics. (7 marks)

Appeared in: S24(7), W22(7)

Ans:

Three modes from V-I curve:

1. **Reverse blocking mode** – Anode negative wrt cathode. J_1 & J_3 reverse biased, J_2 forward biased. Small reverse leakage current flows until reverse breakdown voltage ($V_{\beta r}$). SCR acts as open switch.
2. **Forward blocking mode (off-state)** – Anode positive, gate open. J_2 reverse biased, small forward leakage current. SCR blocks voltage up to **breakover voltage (V_{6o})**.
3. **Forward conduction mode (on-state)** – When V_{ak} exceeds V_{6o} or gate current applied, J_2 avalanches. SCR turns on; voltage drops to ~1-2V (on-state drop). Current limited by external load.

Additional sub-mode: Latching – after trigger, SCR remains on even if gate removed ($I_a > I_l$).

Turn-off – I_a drops below I_h, SCR returns to blocking mode.

[DG PROMPT]

Title: Static V-I Characteristics with Three Modes

Description: Draw X-axis V_{ak} (negative to positive), Y-axis I_a. Mark reverse blocking region (negative V, small negative I) with reverse breakdown knee. Mark forward blocking region (positive V up to V_{6o}, small positive I). Mark forward conduction region (vertical drop to low V, high I). Indicate latching and holding currents. Add a curve for triggered mode (lower V_{6o}).

Real-world application: Used to design phase-controlled rectifiers, AC voltage regulators, and protection circuits.

O3. Explain forward blocking and forward conduction mode of SCR using V-I characteristics. (7 marks)

Appeared in: S22(7)

Ans:

Forward Blocking Mode (off-state):

- Anode positive, gate open. Junctions J_1 & J_3 forward biased, J_2 reverse biased.
- Only small leakage current (μA to mA) flows.
- SCR withstands forward voltage up to **breakover voltage V_{6o}** (typically 100-2000V).
- If $V_{ak} > V_{6o}$, avalanche breakdown at J_2 occurs – unwanted turn-on.

Forward Conduction Mode (on-state):

- Triggered by gate pulse or voltage > V_{6o}.
- J_2 breaks down, holes inject from P_1 into N_1, electrons from N_2 into P_2. Regenerative feedback (two-transistor model) turns SCR fully on.
- Voltage across SCR drops to **on-state voltage (1–2V)**, independent of current.

- SCR behaves like a closed switch; current determined by external circuit.
- SCR remains latched even after gate signal removed (until $I_a < I_h$).

[DG PROMPT]
Title: Forward Blocking and Forward Conduction Modes
Description: Draw only forward quadrant of V-I curve. X-axis V_{ak}, Y-axis I_a. From origin: small upward slope (leakage) then horizontal line to V_{6o}, then vertical drop, then slight upward slope (on-state). Label "Forward blocking region" and "Forward conduction region". Mark V_{6o}, I_l, I_h.
Application: Essential for understanding SCR turn-on mechanisms in inverters and choppers.

O4. Draw and explain any three triggering methods for Thyristors. (7 marks)
Appeared in: S23(7)
Ans:
Three common triggering methods:

1. **Gate Triggering (most common)** – Positive voltage pulse between gate and cathode. Forward biases J_3, injects electrons into P_2, reduces V_{6o}. Simple, precise control.
2. **dv/dt Triggering** – High rate of rise of forward voltage charges junction capacitance (J_2), causing displacement current that triggers SCR. Unwanted; prevented by snubber.
3. **Light Triggering (LTT)** – Light pulse strikes photosensitive gate region. Used in HVDC systems. Electrical isolation, noise immunity.

Other methods: Temperature triggering, voltage breakover, gate turn-off (for GTO).
[DG PROMPT]
Title: Three Thyristor Triggering Methods
Description: Draw three separate small schematics.

- **Gate triggering**: SCR symbol with gate circuit (battery + resistor + switch) connected between gate and cathode.
- **dv/dt triggering**: SCR with parallel capacitor across anode-cathode, series inductor to show transient.
- **Light triggering**: SCR symbol with light arrow falling on gate region.

Real-world application: Gate triggering in phase control (light dimmers), dv/dt suppression in snubber networks, light triggering in HVDC valves.

O5. List various SCR turn on methods. Discuss any one in detail. (4 marks)
Appeared in: S25(4) OR part
Ans:
Turn-on methods:

1. Gate triggering
2. dv/dt triggering
3. Voltage breakover (V_{6o})
4. Temperature triggering
5. Light triggering
6. Gate turn-off (for GTO – but that's turn-off)

Detailed discussion (Gate triggering):

- A positive voltage pulse (typically 3-5V, 10-100µs) applied between gate and cathode.
- Forward biases J_3, injects electrons into P_2, which reach J_2 and cause avalanche.
- Reduces breakover voltage progressively; SCR turns on at lower V_{ak}.
- Advantages: precise control, low gate power (mA level), easy to isolate.

- Gate pulse must exceed **gate trigger current (I_{G_t})** and **gate trigger voltage (V_{G_t})**.

Real-world application: Used in all phase-controlled rectifiers, AC switches, and inverters.

O6. Explain RC firing circuit / R-C triggering / Resistance triggering. (7 marks)
Appeared in: W23(7), W22(3) OR part
Ans:
RC firing circuit (Resistance-Capacitance triggering) – A simple phase control circuit using RC phase shift to trigger SCR at a desired delay angle (α).
Working principle:

- AC supply (V_s) charges capacitor C via variable resistor R.
- Gate-cathode circuit (with DIAC or breakover device) connected across C.
- When capacitor voltage reaches SCR's gate trigger voltage (or DIAC breakover), SCR turns on.
- By varying R, charging time constant $\tau = RC$ changes → firing angle α controlled.

Circuit description:

- Series R from supply to C; parallel R (or pot) to adjust.
- SCR gate connected to C through a small resistor or DIAC.
- Load (R_l) in series with SCR.

Waveforms:

- Supply voltage sine wave.
- Capacitor voltage exponential rise.
- Firing pulse at α where $Vc = V_{G_t}$.

Advantages: Simple, low cost.
Limitations: Poor regulation for varying loads, limited to resistive loads, firing angle range ~0–90°.
Real-world application: Light dimmers, small heater controllers, battery chargers.
[DG PROMPT]
Title: RC Firing Circuit for SCR
Description: Draw AC supply (sine source) connected to series load (R_l) and SCR anode-cathode. From supply, also connect a branch: variable resistor R (potentiometer) in series with capacitor C; junction of R-C connected to SCR gate through a small resistor and optionally a DIAC. Ground reference. Label V_s, R, C, R_l, SCR, gate.

O7. Draw switching characteristics of SCR during turn-on and turn-off. (3 marks)
Appeared in: W23(3)
Ans:
Turn-on waveforms (I_a, V_{ak} vs time):

- **Delay time (t_d)** – gate pulse applied until I_a rises to 10%. V_{ak} starts falling.
- **Rise time (t_r)** – I_a from 10% to 90%; V_{ak} drops sharply.
- **Spread time (t_s)** – conduction spreads across entire junction.
  Total turn-on time $t_{on} = t_d + t_r + t_s$.

Turn-off (reverse recovery):

- **Reverse recovery time (t_{rr})** – after anode current zero, reverse current peak and decay.
- **Gate recovery time** – SCR regains blocking ability.

[DG PROMPT]
Title: Switching Characteristics of SCR (Turn-on and Turn-off)
Description: Two separate time-axis graphs.

- **Turn-on**: X-axis time, Y-axis I_a and V_{ak}. Show gate pulse (I_G). I_a rises from 0 to full; V_{ak} drops from V_{ak} to ~1V. Mark t_d, t_r, t_s.

- **Turn-off**: Show I_a falling to zero, then negative reverse current peak, decaying to zero. Mark t_{rr}.

O8. Explain turn-on and turn-off characteristics of SCR. (4 marks)
Appeared in: W24(4)
Ans:
Turn-on process (gate trigger):

1. **Delay time (t_s)** – 0.5–2 µs. Gate charge builds, J_2 starts conducting.
2. **Rise time (t_r)** – 1–4 µs. Anode current rises, voltage falls.
3. **Spread time (t_s)** – 2–5 µs. Conduction spreads to whole cathode area.

Turn-off process (commutation):

- SCR naturally turns off when anode current falls below **holding current**.
- **Reverse recovery** – stored charges must be removed. Reverse current peak (I_{rr}) and **reverse recovery time (t_{rr})**.
- **Circuit turn-off time ($t_o$ff)** required > device turn-off time to avoid re-triggering.

Factors: t_{on} decreases with higher gate current; $t_o$ff increases with temperature.
Application: Critical for high-frequency inverters and forced commutation circuits.

O9. Discuss the requirement of Snubber circuit for reliable operation of SCR. (4 marks)
Appeared in: S25(4)
Ans:
Snubber circuit – typically an RC network connected across SCR (anode-cathode).
Why required?

1. **dv/dt protection** – Prevents false turn-on due to high rate of rise of forward voltage (dv/dt) across J_2. Snubber capacitor limits dv/dt.
2. **Peak voltage clamping** – Suppresses voltage spikes during turn-off (inductive load commutation). Resistor damps oscillations.
3. **Reduces switching losses** – Shapes voltage/current overlap.

Design basics:

- C ≈ 0.1–1 µF, R ≈ 10–100 Ω (power rated).
- Diode may be added for unidirectional clamping.

Real-world application: Essential in all inductive load circuits (motors, relays, transformers) and AC-DC converters.

O10. Define Holding current, latching current for SCR. (4 marks)
Appeared in: S23(4)
Ans:

- **Latching current (I_l)** – Minimum anode current required immediately after gate trigger to maintain conduction even after gate signal is removed. Typically 1.5 to 2 times holding current.
- **Holding current (I_h)** – Minimum anode current below which SCR turns off (stops conducting) when gate is open. $I_h < I_l$.

Parameter	Condition	Typical value
I_l	After trigger, gate removed	10–100 mA
I_h	Before turn-off, gate open	5–50 mA

Practical significance: I_l must be exceeded for reliable latching; I_h determines turn-off capability in phase control circuits.

O11. Describe the working of UJT Relaxation Oscillator circuit. (7 marks)
Appeared in: S23(3) OR part, W24(7)
Ans:
UJT relaxation oscillator – generates triggering pulses for SCR.
Components: UJT (Unijunction Transistor), resistor R_e, capacitor C, resistors R_1 and R_2, DC supply V_BB.
Working:

1. Initially capacitor C charges through R_e towards V_BB.
2. When capacitor voltage reaches **peak point voltage** $V_p = \eta V\_BB + V_D$ (η = intrinsic standoff ratio, ~0.6), UJT turns on (negative resistance region).
3. Capacitor discharges rapidly through B1 (emitter-base1) and external resistor R_1, producing a sharp voltage pulse across R_1.
4. After discharge, UJT turns off; capacitor recharges. Cycle repeats.

Oscillation frequency: $f \approx 1 / (R_e C \ln(1/(1-\eta)))$.
Output pulses – taken across R_1 (or R_2) to trigger SCR gate.
Advantages: Simple, stable frequency, low cost.
Real-world application: Phase control circuits for AC dimmers, battery chargers, motor speed controls.
[DG PROMPT]
Title: UJT Relaxation Oscillator Circuit
Description: Draw DC supply V_BB positive. Connect R_e from V_BB to emitter of UJT. Connect capacitor C from emitter to ground. UJT base B1 connected to ground through R_1; base B2 connected to V_BB through R_2. Output taken across R_1. Label all components.

O12. Explain pulse transformer and opto-coupler. (4 marks)
Appeared in: W24(4) OR part
Ans:
Pulse transformer:

- Small ferrite-core transformer designed to transfer narrow, high-current pulses to SCR gate.
- Provides electrical isolation between control circuit (low voltage) and power circuit (high voltage).
- Turns ratio typically 1:1 or step-down for current gain.
- Advantages: fast rise time, high noise immunity.

Opto-coupler (optically coupled isolator):

- Contains LED (input side) and phototransistor/photodiode (output side) in same package.
- Input electrical signal modulates light; output side drives SCR gate.
- Provides isolation up to several kV.
- Commonly used ICs: MOC3021, 4N35.

Comparison:

Feature	Pulse Transformer	Opto-coupler
Isolation type	Magnetic	Optical
Pulse width	Narrow (μs)	Any
Cost	Low	Moderate

Real-world application: Both used in microprocessor-based firing circuits for inverters and converters.

O13. Determine 7 important parameters which can be derived from datasheet of SCR. (7 marks)
Appeared in: S22(7) OR part
Ans:
Seven key datasheet parameters for SCR:

1. **VDRM / VRRM** – Repetitive peak off-state forward/reverse voltage (maximum blocking voltage).
2. **IT(RMS)** – RMS on-state current (max continuous current).
3. **ITSM** – Non-repetitive surge current (one cycle).
4. **IGT / VGT** – Gate trigger current and voltage (minimum to turn on).
5. **IH** – Holding current (minimum for latching).
6. **IL** – Latching current.
7. **dv/dt** – Critical rate of rise of off-state voltage (V/μs).

Additional important:

- **tq** – Turn-off time (μs) for fast switching.
- **VTM** – On-state voltage drop at rated current.
- **Rth(j-c)** – Thermal resistance junction to case.

Real-world application: Used to select SCR for given load, snubber design, and heat sink sizing.

O14. Analyze briefly 7 technical parameters required for selection of power electronic switch. (7 marks)
Appeared in: S22(7)
Ans:
While selecting a power switch (SCR, MOSFET, IGBT, etc.), consider:

1. **Voltage rating** – Peak blocking voltage (VDRM) > max circuit voltage + safety margin (20-30%).
2. **Current rating** – RMS or average current with surge handling capability (ITSM).
3. **Switching speed** – Turn-on/off times (ton, toff). MOSFET/IGBT fast (kHz–MHz); SCR slow (50–400Hz).
4. **On-state voltage drop / conduction loss** – Lower VCE(sat) or VDS(on) reduces heat.
5. **Gate drive requirements** – Voltage vs current controlled. MOSFET/IGBT need voltage (VGS), SCR needs current pulse.
6. **dv/dt and di/dt capability** – High dv/dt may false-trigger SCR; high di/dt causes local heating.
7. **Thermal characteristics** – Junction-to-case thermal resistance, max Tj (150-175°C).

Selection guide:

- Low frequency, very high voltage/current → SCR
- Medium frequency, medium power → IGBT
- High frequency, low voltage → MOSFET
- Bidirectional AC switching → TRIAC

Real-world application: Choosing devices for inverters, SMPS, motor drives.

O15. Explain the operation of IGBT using sectional view. (7 marks)
Appeared in: S22(7)
Ans:

IGBT (Insulated Gate Bipolar Transistor) – Combines MOSFET gate and BJT conduction.

Sectional view structure (N-channel IGBT):

- **Collector (P^+ substrate)** – bottom layer.
- **N^+ buffer layer** – reduces punch-through.
- **N^- drift layer** – lightly doped, supports voltage.
- **P-body** – channel region.
- **N^+ source (emitter)** – top layer.
- **Gate** – polysilicon over oxide on P-body.

Operation:

- **Turn-on (positive VGE > threshold):**
  - Inversion layer forms in P-body under gate, connecting N^+ source to N^- drift.
  - Electrons flow from emitter to drift → forward biases P^+ collector/N^- junction → holes inject from collector.
  - Conductivity modulation reduces on-resistance.
- **On-state:** Current flows by both electrons (MOSFET channel) and holes (bipolar injection).
- **Turn-off (VGE = 0):**
  - MOSFET channel closes. Electron current stops.
  - Stored holes recombine or are extracted → tail current (slow turn-off).

Advantages: Low on-state drop, easy gate drive, high input impedance.

Real-world application: Motor drives (elevators, EVs), induction heating, UPS systems.

[DG PROMPT]

Title: Sectional View of IGBT (N-Channel)

Description: Draw vertical cross-section. Top: Emitter metal contacting N^+ and P-body. Gate electrode on top of oxide layer, straddling between N^+ source and N^- drift. Below P-body: N^- drift region, then N^+ buffer, then P^+ collector with collector metal. Label all layers: Emitter, Gate, Collector, N^+ Source, P-Body, N^- Drift, N^+ Buffer, P^+ Collector. Show electron flow path (vertical) and hole injection.

****