GUJARAT TECHNOLOGICAL UNIVERSITY

BE-4 SEMESTER – OLD PAPER – S22 TO W25 – QUESTION BANK ANSWER

Subject Name & Code:

ANALOG CIRCUIT DESIGN (3141002)

(Disclaimer: The purpose of these AI-generated responses is just education and reference. Utilise them to grasp topics and structure, but always rewrite in your own words and double-check)

Unit 5: Timer IC 555 and Phase-Locked Loop (PLL)

Q.1 – Explain the block diagram and working of IC 555 timer.
(7 marks)
Ans:
Block diagram of IC 555 timer:
The 555 timer IC consists of the following functional blocks:

- **Voltage divider:** Three equal resistors (5kΩ each) connected between V_{CC} and ground, producing reference voltages $\frac{2}{3}V_{CC}$ and $\frac{1}{3}V_{CC}$.
- **Two comparators:**
  - **Comparator 1 (Threshold comparator):** Compares threshold voltage (pin 6) with $\frac{2}{3}V_{CC}$.
  - **Comparator 2 (Trigger comparator):** Compares trigger voltage (pin 2) with $\frac{1}{3}V_{CC}$.
- **SR flip-flop:** Set and reset by comparator outputs.
- **Discharge transistor (NPN):** Controlled by flip-flop output (Q_bar). When ON, it discharges external capacitor.
- **Output buffer (inverter):** Provides output current drive.

Pin diagram (8-pin DIP):
1 – GND, 2 – Trigger, 3 – Output, 4 – Reset, 5 – Control Voltage, 6 – Threshold, 7 – Discharge, 8 – V_{CC}.
Diagram prompt:
[DG PROMPT]
Title: Internal block diagram of IC 555 timer
Description: Draw three equal resistors (5k each) in series from Vcc (pin 8) to ground (pin 1). Tap the node between first and second resistor as $\frac{2}{3}V_{CC}$ to non-inverting input of Comparator 1. Tap between second and third as $\frac{1}{3}V_{CC}$ to inverting input of Comparator 2. Comparator 1: inverting input connected to Threshold pin (pin 6). Comparator 2: non-inverting input connected to Trigger pin (pin 2). Outputs of comparators go to SR flip-flop: Comparator 1 output to Reset, Comparator 2 output to Set. Flip-flop output (Q) goes to output buffer (inverter) to pin 3. Flip-flop complementary output (Q_bar) drives base of discharge transistor (NPN) whose collector is pin 7 (Discharge) and emitter to ground. Reset pin (pin 4) connected to flip-flop reset (active low). Control Voltage pin (pin 5) connected to the $\frac{2}{3}V_{CC}$ node (via a voltage follower internally). Label all pins.
Working principle:

1. **Voltage divider** provides fixed reference voltages of $\frac{1}{3}V_{CC}$ and $\frac{2}{3}V_{CC}$ regardless of V_{CC} (within limits).
2. **Trigger comparator (Comp 2):** When trigger voltage (pin 2) falls below $\frac{1}{3}V_{CC}$, Comp 2 output goes high → sets the SR flip-flop → output (pin 3) goes high, and discharge transistor turns OFF.
3. **Threshold comparator (Comp 1):** When threshold voltage (pin 6) rises above $\frac{2}{3}V_{CC}$, Comp 1 output goes high → resets SR flip-flop → output goes low, and discharge transistor turns ON (pin 7 connected to ground).
4. **Reset pin (pin 4):** When pulled low (0V), it forces flip-flop reset → output low, transistor ON.
5. **Control voltage pin (pin 5):** Allows external adjustment of the $\frac{2}{3}V_{CC}$ reference (modulates timing).

Operating modes:

- **Astable mode:** Free-running oscillator (no stable state).
- **Monostable mode:** One-shot pulse generator.
- **Bistable mode (Schmitt trigger):** Two stable states.

Real-world application: 555 timers are used in pulse generation, time delay, LED flashers, tone generators, PWM controllers, and missing pulse detectors.

Q.2 – Explain monostable multivibrator using IC 555.
(7 marks)
Ans:
Definition: A monostable multivibrator (one-shot) produces a single output pulse of fixed duration when triggered. It has one stable state (output LOW) and one quasi-stable state (output HIGH).
Circuit connections (555 in monostable mode):

- Connect V_{CC} to pin 8, GND to pin 1.
- Reset pin (4) tied to V_{CC} (disable reset).
- Control voltage pin (5) grounded via 0.01µF capacitor (noise bypass).
- External resistor R from V_{CC} to pin 7 (Discharge).
- External capacitor C from pin 6 (Threshold) to ground.
- Pin 6 and pin 7 connected together (short).
- Trigger input applied to pin 2.
- Output taken from pin 3.

Diagram prompt:
[DG PROMPT]
Title: 555 timer monostable multivibrator circuit
Description: Draw IC 555 with pin numbers. Connect pin 8 to Vcc, pin 1 to ground. Connect pin 4 to Vcc. Connect pin 5 to ground via 0.01µF capacitor. Connect resistor R from Vcc to pin 7. Connect capacitor C from pin 6 to ground, and also connect pin 7 to pin 6 (short). Trigger input (active low pulse) to pin 2. Output at pin 3. Show waveform: trigger pulse (negative spike), output pulse width T = 1.1 RC, capacitor voltage charging exponential from 0 to $\frac{2}{3}V_{CC}$.
Working principle (step-by-step):

1. **Stable state (output LOW):** Initially, trigger pin 2 is HIGH (above $\frac{1}{3}V_{CC}$). SR flip-flop is reset, output LOW, discharge transistor ON → pin 7 at ground → capacitor C fully discharged (0V).

2. **Triggering (negative pulse):** A negative trigger pulse applied to pin 2 brings it below $\frac{1}{3}V_{CC}$. Comparator 2 output goes HIGH → sets flip-flop → output goes HIGH, discharge transistor turns OFF.
3. **Timing phase (quasi-stable):** Transistor OFF, capacitor C charges through resistor R from V_{CC} with time constant $\tau = RC$. Voltage across C rises exponentially.
4. **Threshold detection:** When capacitor voltage reaches $\frac{2}{3}V_{CC}$, Comparator 1 output goes HIGH → resets flip-flop → output goes LOW, discharge transistor turns ON.
5. **Discharge:** Transistor ON rapidly discharges C to 0V. Circuit returns to stable state, waiting for next trigger.

Important: The trigger pulse must be shorter than the output pulse width. The circuit is **non-retriggerable** (additional triggers during timing have no effect).
Output pulse width formula:

$$\boxed{T = 1.1 \times R \times C}$$

(The factor 1.1 comes from ln (3) ≈ 1.0986.)
Numerical example: For $R = 10k\Omega$, $C = 100\mu F$, $T = 1.1 \times 10^4 \times 10^{-4} = 1.1$ seconds.
Applications:

- Debouncing mechanical switches
- Pulse stretcher
- Delay timers
- Missing pulse detector (with retriggerable monostable)

Q.3 – Explain astable multivibrator using timer IC.
(7 marks)
Ans:
Definition: An astable multivibrator is a free-running oscillator that produces a continuous square wave without any external trigger. The 555 timer in astable mode has no stable state – it continuously switches between HIGH and LOW.
Circuit connections (555 in astable mode):

- V_{CC} to pin 8, GND to pin 1.
- Reset pin (4) to V_{CC}.
- Control voltage pin (5) grounded via 0.01µF capacitor.
- Two resistors: R_1 from V_{CC} to pin 7 (Discharge), R_2 from pin 7 to pin 6 (Threshold) and also to pin 2 (Trigger).
- Capacitor C from pin 6 (and pin 2) to ground.
- Output from pin 3.

Diagram prompt:
[DG PROMPT]
Title: 555 timer astable multivibrator circuit
Description: Draw IC 555. Connect pin 8 to Vcc, pin 1 to ground, pin 4 to Vcc, pin 5 to ground via 0.01µF. Connect resistor R1 from Vcc to pin 7. Connect resistor R2 from pin 7 to pin 6. Connect pin 6 to pin 2 (short). Connect capacitor C from pin 6 to ground. Output at pin 3. Show waveforms: capacitor voltage charging from $\frac{1}{3}V_{CC}$ to $\frac{2}{3}V_{CC}$ and discharging from $\frac{2}{3}V_{CC}$ to $\frac{1}{3}V_{CC}$; output square wave with period T = T1 + T2.
Working principle (step-by-step):

1. **Initial assumption:** Assume capacitor C initially discharged (0V). Output (pin 3) is HIGH, discharge transistor (pin 7) is OFF.
2. **Charging phase (T1):** Capacitor C charges through $R_1 + R_2$ toward V_{CC}. Voltage

rises exponentially.

3. **Threshold reaching $\frac{2}{3}V_{CC}$:** Comparator 1 triggers → resets flip-flop → output goes LOW, discharge transistor turns ON (pin 7 connected to ground).
4. **Discharging phase (T2):** Capacitor discharges through R_2 only (since pin 7 is ground, R_1 is bypassed). Voltage falls exponentially.
5. **Trigger reaching $\frac{1}{3}V_{CC}$:** Comparator 2 triggers → sets flip-flop → output goes HIGH, discharge transistor turns OFF.
6. Cycle repeats indefinitely.

Timing equations:

- **Charging time (output HIGH):**

$$T_1 = 0.693(R_1 + R_2)C$$

- **Discharging time (output LOW):**

$$T_2 = 0.693(R_2)C$$

- **Total period:**

$$T = T_1 + T_2 = 0.693(R_1 + 2R_2)C$$

- **Frequency:**

$$f = \frac{1}{T} = \frac{1.44}{(R_1 + 2R_2)C}$$

- **Duty cycle:**

$$D = \frac{T_1}{T} = \frac{R_1 + R_2}{R_1 + 2R_2} \times 100\%$$

Duty cycle < 50%: To achieve duty cycle less than 50%, add a diode in parallel with R_2 (anode to pin 7, cathode to pin 6) so that charging path is only through R_1 and discharging through R_2.

Numerical example:

Given $R_1 = 1k\Omega$, $R_2 = 10k\Omega$, $C = 0.1\mu F$.

$T_1 = 0.693(11k)(0.1\mu) = 0.7623\ ms$, $T_2 = 0.693(10k)(0.1\mu) = 0.693\ ms$,

$f = 1.44/(1k + 20k) \times 0.1\mu = 1.44/(2.1k \times 0.1\mu) = 1.44/0.00021 = 6.857\ kHz$.

Applications:

- Clock pulse generator
- LED flasher
- Tone generator (buzzer)
- PWM generation (with duty cycle control)

Q.4 – Explain the block diagram of PLL and briefly explain its operation. (7 marks)

Ans:

Phase-Locked Loop (PLL) is a feedback control system that locks the output frequency of a voltage-controlled oscillator (VCO) to the frequency of an input reference signal.

Block diagram of PLL:

A basic PLL consists of four functional blocks:

Block	Function

Block	Function
Phase Detector (PD)	Compares phase of input signal f_{in} and VCO output f_{out}, produces an error voltage proportional to phase difference.
Loop Filter (LPF)	Low-pass filter removes high-frequency components and noise from PD output, provides a DC control voltage.
Voltage-Controlled Oscillator (VCO)	Generates output frequency proportional to control voltage.
Amplifier (optional)	Amplifies the filtered error voltage to drive the VCO.

Diagram prompt:
[DG PROMPT]
Title: Block diagram of Phase-Locked Loop (PLL)
Description: Draw four rectangular blocks in sequence, with feedback. Start with input signal f_{in} to a circle labeled "Phase Detector". Second block "Loop Filter (LPF)", third block "VCO". Output of VCO is f_{out}. Feedback path: VCO output connects back to the Phase Detector (second input). Also output f_{out} is the final PLL output. Add an optional "Amplifier" between LPF and VCO. Label error voltage V_e after PD, V_c (control voltage) after LPF.

Operation (step-by-step):

1. **Free-running state:** When input signal f_{in} is absent or out of lock, the VCO runs at its free-running frequency f_o (center frequency).
2. **Capture process:** When f_{in} is applied, the phase detector compares f_{in} and f_{out}. The output is a voltage that varies with phase difference. This voltage passes through the loop filter to become V_c, which adjusts the VCO frequency toward f_{in}.
3. **Lock state:** When $f_{out} = f_{in}$ (and phase difference is constant), the phase detector output becomes a steady DC voltage (or periodic with average DC). The loop filter smooths it, and VCO stays locked.
4. **Phase lock:** The phase difference is not zero but a small constant offset needed to produce the required control voltage.

Important parameters:

- **Lock range (hold-in range):** Frequency range over which PLL can maintain lock once acquired.
- **Capture range (pull-in range):** Frequency range over which PLL can acquire lock from an unlocked state.
- **Lock-in time:** Time taken to achieve lock.

Types of Phase Detectors:

- **Analog multiplier (Gilbert cell):** For sinusoidal signals.
- **Exclusive-OR gate:** For square waves.
- **Phase-frequency detector (PFD):** For wide capture range, used in digital PLLs.

Applications:

- Frequency synthesis (clock generation)
- FM demodulation
- Frequency multiplication/division
- Clock recovery in data communication
- Motor speed control

Real-world application: PLLs are used in microcontrollers (PLL clock multiplier), radio receivers (local oscillator), and CD/DVD drives (data clock recovery).

Q.5 – What is PLL? Explain operation with basic blocks and mention four applications in radio communication.
(4 marks)
Appeared in: S25 (Q2b)
Ans:
Phase-Locked Loop (PLL) is an electronic feedback circuit that synchronizes the output frequency of a voltage-controlled oscillator (VCO) with the frequency of an input reference signal.
Basic blocks and operation:

- **Phase Detector (PD):** Compares the phase difference between input signal f_{in} and VCO output f_{out}, produces an error voltage.
- **Loop Filter (LPF):** Low-pass filter removes high-frequency components, outputs a DC control voltage.
- **VCO:** Generates output frequency proportional to the control voltage.
- **Feedback loop:** VCO output is fed back to PD. When locked, $f_{out} = f_{in}$ with constant phase difference.

Four applications in radio communication:

1. **FM demodulation** – Recovering audio from FM signals.
2. **Frequency synthesis** – Generating stable local oscillator frequencies for receivers/transmitters.
3. **Clock recovery** – Extracting timing from serial data streams (e.g., in digital radio).
4. **Frequency multiplication/division** – Generating harmonics for up/down conversion.

Q.6 – Draw block diagram of PLL and briefly explain its operation.
(7 marks)
Appeared in: S23 (Q4b, 4 marks), S22 (Q3c, 7 marks) → Highest 7 marks
Ans:
Block diagram of PLL:
[DG PROMPT]
Title: Block diagram of Phase-Locked Loop (PLL)
Description: Draw four functional blocks in sequence with a feedback path.

- Block 1 (left): Phase Detector (PD) – circle with inputs: arrow from input f_{in} and arrow from VCO output. Output arrow to Block 2.
- Block 2: Loop Filter (LPF) – low-pass filter symbol. Output arrow to Block 3.
- Block 3: Voltage-Controlled Oscillator (VCO) – output arrow to f_{out}.
- Feedback: From VCO output back to PD (second input).
- Label: Error voltage V_e after PD, Control voltage V_c after LPF. Optional amplifier between LPF and VCO.

Operation (brief):

1. **Free-running state:** No input or unlocked – VCO runs at center frequency f_o.
2. **Capture:** Input f_{in} applied – PD produces an error voltage proportional to phase difference. LPF filters it to DC control voltage, which pulls VCO frequency toward f_{in}.
3. **Lock:** When $f_{out} = f_{in}$, the phase difference is constant, producing a steady control voltage. The PLL remains locked if input frequency changes slowly within lock range.
4. **Hold-in range:** Frequency range over which lock is maintained.

5. **Capture range:** Frequency range over which lock can be acquired.

Real-world application: PLLs are used in frequency synthesizers (e.g., in mobile phones for channel selection), FM demodulators, and clock multipliers in microprocessors.

Q.7 – Design a monostable multivibrator for $T_P = 11\ \mu s, C = 0.01\ \mu F$.
(3 marks)
Appeared in: W25 (Q5a)
Ans:
Given:

$$T_P = 11\ \mu s = 11 \times 10^{-6}\ s$$
$$C = 0.01\ \mu F = 0.01 \times 10^{-6} = 10^{-8}\ F$$

Formula: For 555 monostable, $T_P = 1.1 \times R \times C$
Solution:

$$R = \frac{T_P}{1.1 \times C} = \frac{11 \times 10^{-6}}{1.1 \times 10^{-8}} = \frac{11}{1.1} \times 10^2 = 10 \times 100 = 1000\ \Omega = 1\ k\Omega$$

Final Answer:

$$\boxed{R = 1\ k\Omega}$$

(Use standard resistor value: 1 kΩ.)

Q.8 – Design a monostable multivibrator using timer IC for $T_P = 11\ \mu s, C = 0.1\ \mu F$.
(3 marks)
Appeared in: W22 (Q5a)
Ans:
Given:

$$T_P = 11\ \mu s = 11 \times 10^{-6}\ s$$
$$C = 0.1\ \mu F = 0.1 \times 10^{-6} = 10^{-7}\ F$$

Formula: $T_P = 1.1 \times R \times C$
Solution:

$$R = \frac{T_P}{1.1 \times C} = \frac{11 \times 10^{-6}}{1.1 \times 10^{-7}} = \frac{11}{1.1} \times 10^1 = 10 \times 10 = 100\ \Omega$$

Final Answer:

$$\boxed{R = 100\ \Omega}$$

(Use 100 Ω resistor.)

Q.9 – Design an astable multivibrator using IC 555 for $T = 50\%$ duty cycle, $F = 10\ kHz, C = 0.01\ \mu F$.
(4 marks)
Appeared in: W25 (Q5b)
Ans:
Given:
Duty cycle $D = 50\% \rightarrow T_1 = T_2 \rightarrow$ Charging time = Discharging time.
For 50% duty cycle, need $R_1 = 0$ (or use diode configuration). Standard circuit with diode: Connect a diode in parallel with R_2 (anode to pin 7, cathode to pin 6). Then charging path is only through R_1, discharging through R_2. For 50% duty cycle, set $R_1 = R_2$.
Frequency $f = 10\ kHz = 10^4\ Hz$

$$C = 0.01\ \mu F = 10^{-8}\ F$$

Formula (with diode):

$T_1 = 0.693 R_1 C, T_2 = 0.693 R_2 C$

$$f = \frac{1}{T_1 + T_2} = \frac{1}{0.693(R_1 + R_2)C}$$

For $R_1 = R_2 = R$, $f = \frac{1}{0.693 \times 2RC}$

Solution:

$$R = \frac{1}{0.693 \times 2 \times f \times C} = \frac{1}{0.693 \times 2 \times 10^4 \times 10^{-8}} = \frac{1}{0.693 \times 2 \times 10^{-4}} = \frac{1}{1.386 \times 10^{-4}} \approx 7215\ \Omega$$

Choose $R = 7.2\ k\Omega$ (standard).

Final Answer:

$$\boxed{R_1 = R_2 \approx 7.2\ k\Omega,\ C = 0.01\ \mu F}$$

(Use diode 1N4148 across R_2.)

Q.10 – Design an astable multivibrator using IC 555 for 75% duty cycle, $F = 1\ kHz$, $C = 0.1\ \mu F$.

(4 marks)

Appeared in: W22 (Q5b)

Ans:

Given:

Duty cycle $D = 75\% = T_1/(T_1 + T_2) = 0.75 \rightarrow T_1 = 3T_2$

$f = 1\ kHz \rightarrow T = 1\ ms$

$$C = 0.1\ \mu F = 10^{-7}\ F$$

Formulas (without diode):

$$T_1 = 0.693(R_1 + R_2)C$$
$$T_2 = 0.693 R_2 C$$
$$T = 0.693(R_1 + 2R_2)C = 1\ ms$$

Also $\frac{T_1}{T} = \frac{R_1 + R_2}{R_1 + 2R_2} = 0.75$

Let $k = R_2/R_1$. Then $\frac{1+k}{1+2k} = 0.75 \rightarrow 1 + k = 0.75 + 1.5k \rightarrow 0.25 = 0.5k \rightarrow k = 0.5$.

So $R_2 = 0.5R_1$.

Now $T = 0.693(R_1 + 2 \times 0.5R_1)C = 0.693(R_1 + R_1)C = 0.693 \times 2R_1C = 1.386R_1C = 10^{-3}$

$$R_1 = \frac{10^{-3}}{1.386 \times 10^{-7}} = \frac{10^{-3}}{1.386 \times 10^{-7}} = \frac{10^4}{1.386} \approx 7215\ \Omega$$
$$R_2 = 0.5 \times 7215 \approx 3607\ \Omega$$

Final Answer:

$$\boxed{R_1 \approx 7.2\ k\Omega,\ R_2 \approx 3.6\ k\Omega,\ C = 0.1\ \mu F}$$

Q.11 – Given $R_1 = 10\ k\Omega,\ R_2 = 50\ k\Omega,\ C = 0.01\ \mu F$, calculate output frequency and duty cycle of 555 astable multivibrator.

(3 marks)

Appeared in: S23 (Q5a)

Ans:

Given:

$$R_1 = 10\ k\Omega = 10 \times 10^3\ \Omega$$
$$R_2 = 50\ k\Omega = 50 \times 10^3\ \Omega$$
$$C = 0.01\ \mu F = 10^{-8}\ F$$

Formulas:

$$T_1 = 0.693(R_1 + R_2)C$$
$$T_2 = 0.693 R_2 C$$
$$T = T_1 + T_2 = 0.693(R_1 + 2R_2)C$$
$$f = 1/T$$
$$D = T_1/T \times 100\%$$

Solution:

$$T_1 = 0.693(10k + 50k) \times 10^{-8} = 0.693 \times 60 \times 10^3 \times 10^{-8} = 0.693 \times 60 \times 10^{-5}$$
$$= 0.693 \times 0.0006 = 4.158 \times 10^{-4}\ s = 0.4158\ ms$$
$$T_2 = 0.693 \times 50k \times 10^{-8} = 0.693 \times 50 \times 10^{-5} = 0.693 \times 0.0005 = 3.465 \times 10^{-4}\ s$$
$$= 0.3465\ ms$$
$$T = 0.4158 + 0.3465 = 0.7623\ ms$$
$$f = 1/(0.7623 \times 10^{-3}) = 1312\ Hz \approx 1.31\ kHz$$
$$D = \frac{0.4158}{0.7623} \times 100\% = 54.55\%$$

Final Answer:

$$\boxed{f \approx 1.31\ kHz, D \approx 54.55\%}$$

Q.12 – Design an astable multivibrator with ~1 kHz using given components: resistors (2.2k, 3.9k, 4.7k), 0.1µF cap, IC555.
(7 marks)
Appeared in: W23 (Q1c)
Ans:
Given: Available resistors: 2.2 kΩ, 3.9 kΩ, 4.7 kΩ; Capacitor $C = 0.1\ \mu F = 10^{-7}\ F$; Target frequency $f \approx 1\ kHz$.
Objective: Choose R_1 and R_2 from available values to achieve f as close as possible to 1 kHz.
Formula for 555 astable (without diode):

$$f = \frac{1.44}{(R_1 + 2R_2)C}$$
$$R_1 + 2R_2 = \frac{1.44}{fC} = \frac{1.44}{10^3 \times 10^{-7}} = \frac{1.44}{10^{-4}} = 14400\ \Omega = 14.4\ k\Omega$$

We need $R_1 + 2R_2 = 14.4\ k\Omega$, using available resistor values (2.2k, 3.9k, 4.7k). Try combinations:

Combination	R_1 (kΩ)	R_2 (kΩ)	$R_1 + 2R_2$ (kΩ)	f (kHz)
2.2, 2.2	2.2	2.2	2.2 + 4.4 = 6.6	1.44/(6.6e3*1e-7)=2.18
2.2, 3.9	2.2	3.9	2.2 + 7.8 = 10.0	1.44/(10e3*1e-7)=1.44
2.2, 4.7	2.2	4.7	2.2 + 9.4 = 11.6	1.44/(11.6e3*1e-7)=1.24

Combination	R_1 (kΩ)	R_2 (kΩ)	$R_1 + 2R_2$ (kΩ)	f (kHz)
3.9, 2.2	3.9	2.2	3.9 + 4.4 = 8.3	1.44/0.00083=1.73
3.9, 3.9	3.9	3.9	3.9 + 7.8 = 11.7	1.44/0.00117=1.23
3.9, 4.7	3.9	4.7	3.9 + 9.4 = 13.3	1.44/0.00133=1.08
4.7, 2.2	4.7	2.2	4.7 + 4.4 = 9.1	1.44/0.00091=1.58
4.7, 3.9	4.7	3.9	4.7 + 7.8 = 12.5	1.44/0.00125=1.15
4.7, 4.7	4.7	4.7	4.7 + 9.4 = 14.1	1.44/0.00141=1.02

Best choice: $R_1 = 4.7\ k\Omega,\ R_2 = 4.7\ k\Omega$ gives $f \approx 1.02\ kHz$ (closest to 1 kHz).
Alternatively, $R_1 = 3.9\ k\Omega,\ R_2 = 4.7\ k\Omega$ gives 1.08 kHz.
Final design:

$$\boxed{R_1 = 4.7\ k\Omega, R_2 = 4.7\ k\Omega, C = 0.1\ \mu F}$$

Expected frequency ≈ 1.02 kHz.
Circuit: Standard 555 astable with pin connections as per Q.3.

Q.13 – Explain applications of astable multivibrator using timer IC. (7 marks)
Appeared in: W25 (Q5c)
Ans:
The IC 555 in **astable mode** generates a continuous square wave and has numerous applications:
1. Clock pulse generator

- Used in digital circuits (microcontrollers, counters, shift registers) as a timing source.
- Frequency can be adjusted by varying R_1, R_2, C.

2. LED flasher / Blinker

- Drives LEDs at desired flash rate (e.g., 1 Hz for indicator).
- Duty cycle can be set to control brightness.

3. Tone generator (Buzzer driver)

- Produces audio frequencies (200 Hz – 10 kHz) to drive a speaker or piezo buzzer.
- Used in alarms, timers, electronic metronomes.

4. Pulse Width Modulation (PWM) generator

- By adding a diode across R_2, duty cycle can be varied from <50% to >50%.
- Applications: DC motor speed control, LED dimming, servo motor control.

5. Frequency shift keying (FSK) generator

- Two different frequencies generated by switching another resistor in parallel with R_2.
- Used in low-cost data transmission (e.g., DTMF tones).

6. Missing pulse detector (with retriggerable monostable, but astable can be used as a reference)

- Astable provides a reference clock; missing input pulse triggers an alarm.

7. Voltage-controlled oscillator (VCO)

- By applying a control voltage to pin 5, the frequency varies.
- Used in PLLs, function generators.

8. Capacitance / Inductance meter

- Frequency of astable changes with external C or L; measure frequency to determine value.

Real-world example: A 555 astable with $f = 1\ kHz$ and 50% duty cycle can be used to drive a small DC motor with a transistor switch for speed control via PWM.

Q.14 – Write short note on voltage regulator.
(4 marks)
Appeared in: W25 (Q5b), W22 (Q5b), S23 (Q4a) → Highest 4 marks
Ans:
Voltage regulator is an electronic circuit that maintains a constant output voltage regardless of variations in input voltage or load current.
Functions:

- **Line regulation:** Rejects input voltage fluctuations (e.g., ripple from rectifier).
- **Load regulation:** Keeps output voltage stable when load current changes.
- **Output voltage setting:** Provides fixed or adjustable DC voltage.
- **Protection:** Includes overcurrent, short-circuit, and thermal shutdown.

Types of voltage regulators:

Type	Examples	Features
Linear series regulator	78XX, LM317	Low noise, simple, but inefficient for high I/O differential
Linear shunt regulator	Zener + transistor	Used for low power, reference
Switching regulator	Buck, Boost, Buck-boost	High efficiency (80–95%), more complex, noisy
Three-terminal fixed	7805 (+5V), 7912 (-12V)	Easy to use, requires input/output capacitors
Three-terminal adjustable	LM317 (positive), LM337 (negative)	Output set by two resistors

Key parameters:

- Output voltage tolerance (±2% to ±5%)
- Dropout voltage (minimum input-output difference)
- Quiescent current
- Ripple rejection (PSRR)

Real-world application: Every DC power supply (wall adapter, bench supply, battery charger) uses a voltage regulator. 7805 is common in microcontroller projects to step down 9V–12V to 5V.

Q.15 – What is a voltage regulator? List types.
(3 marks)
Appeared in: S23 (Q4a)
Ans:
Voltage regulator is a circuit that automatically maintains a constant output voltage despite changes in input voltage or load current.

Types of voltage regulators:

1. **Based on operation mode:**
   - Linear regulator (series or shunt)
   - Switching regulator (buck, boost, buck-boost, Cuk)
2. **Based on output polarity:**
   - Positive voltage regulators (78XX series)
   - Negative voltage regulators (79XX series)
3. **Based on adjustability:**
   - Fixed voltage regulators (e.g., 7805, 7812)
   - Adjustable voltage regulators (e.g., LM317, LM338)
4. **Based on application:**
   - Low dropout regulators (LDO)
   - High voltage regulators
   - Precision reference (TL431)

Q.16 – Explain simple op-amp voltage regulator, three-terminal regulators (78XX, LM317), heat sink, dual power supply.
(7 marks) *(from syllabus – provide comprehensive answer)*
Ans:
A. Simple op-amp voltage regulator (series pass):

- **Circuit:** Op-amp as error amplifier, Zener diode as reference, pass transistor (BJT/MOSFET) in series with load.
- **Operation:** Output voltage sampled by voltage divider and compared to Zener reference. Op-amp amplifies the error and drives the pass transistor to keep output constant.
- **Output voltage:** $V_o = V_{ref} \times (1 + R_2/R_1)$.

B. Three-terminal fixed regulators (78XX series):

- **78XX:** Positive voltage regulators (7805 = +5V, 7812 = +12V).
- **79XX:** Negative voltage regulators (7905 = -5V).
- **Pinout (TO-220):** Input, Ground, Output.
- **Typical application:** Connect input and output capacitors (0.33µF at input, 0.1µF at output) for stability.
- **Features:** Built-in overcurrent protection, thermal shutdown, safe-area protection.

C. Three-terminal adjustable regulator (LM317):

- **LM317** – positive adjustable regulator (1.25V to 37V).
- **Pinout:** Adjust, Output, Input (TO-220).
- **Output voltage formula:** $V_o = 1.25 \times (1 + R_2/R_1) + I_{adj}R_2$. Typically $I_{adj} \approx 100\mu A$ and $R_1 = 240\Omega$.
- **Application circuit:** R_1 between Output and Adjust, R_2 from Adjust to ground.

D. Heat sink:

- **Purpose:** Dissipate heat generated by the regulator (power loss $P = (V_{in} - V_o) \times I_L$).
- **Material:** Aluminum (extruded or stamped).
- **Thermal resistance** θ_{JA} determines temperature rise.
- **Selection:** Ensure junction temperature $T_j < 150°C$.
- **Installation:** Use thermal grease or insulating pad.

E. Dual power supply:

- Provides both positive and negative regulated voltages (e.g., ±12V for op-amps).
- **Construction:** Use a center-tapped transformer, full-wave rectifier, then 7812 (positive) and 7912 (negative) regulators.
- **Common ground:** Connect the common terminal of both regulators together.

Diagram prompt (dual supply):
[DG PROMPT]
Title: Dual power supply using 7812 and 7912
Description: Draw center-tapped transformer secondary. Two diodes for positive half and two for negative? Better: Full-wave rectifier with center tap as ground. Positive output to 7812 (Input), negative output to 7912 (Input). Ground common. 7812 Output gives +12V, 7912 Output gives -12V. Add capacitors on input and output of each regulator.

Q.17 – Design an adjustable voltage regulator using LM317 for $V_o = 5\ to\ 12V$, $I_o = 1A$, $I_{adj} = 100\mu A$, $R_1 = 240\Omega$.
(7 marks)
Appeared in: W23 (Q5c)
Ans:
Given:
Output range: $V_{o(min)} = 5V$, $V_{o(max)} = 12V$
Load current $I_o = 1A$ (max)

$$I_{adj} = 100\mu A = 10^{-4}A$$

$R_1 = 240\Omega$ (connected between Output and Adjust pins)
Formula for LM317:

$$V_o = 1.25\left(1+\frac{R_2}{R_1}\right) + I_{adj}R_2$$

where $V_{ref} = 1.25V$ (internal reference).
Step 1: Find R_2 for $V_o = 5V$

$$5 = 1.25\left(1+\frac{R_2}{240}\right) + 10^{-4}R_2$$
$$5 - 1.25 = 1.25 \times \frac{R_2}{240} + 10^{-4}R_2$$
$$3.75 = \frac{1.25}{240}R_2 + 0.0001R_2 = (0.0052083 + 0.0001)R_2 = 0.0053083R_2$$
$$R_2 = \frac{3.75}{0.0053083} \approx 706\ \Omega$$

Step 2: Find R_2 for $V_o = 12V$

$$12 = 1.25\left(1+\frac{R_2}{240}\right) + 10^{-4}R_2$$
$$12 - 1.25 = \frac{1.25}{240}R_2 + 0.0001R_2$$
$$10.75 = 0.0053083R_2$$
$$R_2 = \frac{10.75}{0.0053083} \approx 2025\ \Omega$$

Step 3: Select practical potentiometer
Use a potentiometer R_2 variable from about 700Ω to 2025Ω. Standard value: 2.5 kΩ (or 2.2 kΩ + series resistor). For continuous adjustment, use a 2 kΩ pot in series with a fixed 220Ω to get range ~220Ω to 2220Ω.
Step 4: Additional components

- Input capacitor $C_{in} = 0.33\mu F$ (ceramic)
- Output capacitor $C_{out} = 1\mu F$ (tantalum or electrolytic)
- Protection diode across input-output (1N4007)

- Heat sink for LM317 (power dissipation $P = (V_{in} - V_o) \times I_o$, choose V_{in} at least 15V for 12V output)

Final Answer:

$$\boxed{R_1 = 240\Omega, R_2 \approx 700\ \Omega \text{ to } 2025\ \Omega \text{ (use 2.5k pot)}}$$

Q.18 – Explain the design of LM317-based voltage regulator with example. (7 marks)

Appeared in: W24 (Q5c)

Ans:

Design procedure for LM317 adjustable voltage regulator:

Step 1: Determine required output voltage range

Example: Design a regulator to output $V_o = 9V$ at 1A.

Step 2: Choose R_1 value

LM317 datasheet recommends $R_1 = 240\Omega$ (or 120Ω for higher output current). R_1 sets the minimum load current.

Step 3: Calculate R_2 using formula

$$V_o = 1.25\left(1+\frac{R_2}{R_1}\right) + I_{adj}R_2$$

Neglect I_{adj} for first approximation (error < 1%):

$$9 \approx 1.25\left(1+\frac{R_2}{240}\right) \implies \frac{9}{1.25} = 1 + \frac{R_2}{240} \implies 7.2 = 1 + \frac{R_2}{240} \implies \frac{R_2}{240} = 6.2 \implies R_2 = 1488\ \Omega$$

Use standard 1.5 kΩ.

Step 4: Select components

- $C_{in} = 0.33\mu F$ (ceramic) close to input pins
- $C_{out} = 1\mu F$ (tantalum) at output
- Protection diode D_1 from output to input (in case of shorted input)
- Protection diode D_2 from adjust to output (prevents capacitor discharge into adjust pin)

Step 5: Heat sink calculation

Power dissipation $P = (V_{in} - V_o)I_o$. Choose $V_{in} \approx V_o + 3V = 12V$ (dropout ~2V, plus safety).

$P = (12 - 9) \times 1 = 3W$.

Thermal resistance θ_{JA} of LM317 (TO-220) without heatsink ~ 65°C/W → temperature rise 195°C (exceeds 125°C). Need heatsink.

Required θ_{HS}: $T_j - T_a = P \times (\theta_{JC} + \theta_{CS} + \theta_{SA})$. For $T_j = 125°C, T_a = 40°C, \theta_{JC} \approx 3°C/W, \theta_{CS} \approx 1°C/W$:

$85 = 3 \times (3 + 1 + \theta_{SA}) \Rightarrow \theta_{SA} \approx 24°C/W$. Use a small clip-on heatsink.

Example design summary:

- $R_1 = 240\Omega$, $R_2 = 1.5\ k\Omega$ (fixed) for 9V output. For adjustable, use 2.5k pot.
- Input voltage: 12V DC (from rectified transformer).
- Capacitors: $C_{in} = 0.33\mu F$, $C_{out} = 1\mu F$, $C_{adj} = 10\mu F$ (improves ripple rejection).
- Heatsink: TO-220 heatsink with $\theta_{SA} < 25°C/W$.

Final Answer: LM317 with $R_1 = 240\Omega, R_2 = 1.5k\Omega$ gives $V_o \approx 9V$.

Q.19 – What are advantages of adjustable over fixed voltage regulators?

(3 marks)
Appeared in: S22 (Q3a OR)
Ans:
Advantages of adjustable voltage regulators (e.g., LM317) over fixed regulators (e.g., 7805):

1. **Versatility** – One device can produce any output voltage within its range (1.25V to 37V) by changing two external resistors.
2. **Higher output voltage** – Fixed regulators are limited to standard values (5V, 12V, 15V). Adjustable can provide non-standard voltages (e.g., 8.5V, 14.2V).
3. **Better regulation** – Adjustable regulators often have lower temperature coefficient and tighter line/load regulation.
4. **Programmable** – Can be used as current source, battery charger, or with external pass transistor for higher current.
5. **Floating operation** – The LM317 can regulate high voltages (up to 37V differential) independent of ground.
6. **Lower dropout voltage** – Some adjustable LDOs (e.g., LM1085) have lower dropout than fixed 78xx series.

Disadvantage: Requires two external resistors and optionally a potentiometer, increasing component count.

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