GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER–1 PAPER SOLUTION – WINTER 2024

Subject Name & Code:
Basic Electronics Engineering- 3110016

Marks

Q.1 (a) Sketch the characteristics of ideal diode and approximate characteristics of practical diodes. Briefly explain it. **03**

Answer:

Characteristics of Ideal and Practical Diode

🔹 **Ideal Diode Characteristics:**

An **ideal diode** is a theoretical device that acts as a **perfect conductor** when forward-biased and a **perfect insulator** when reverse-biased.

Graphical Representation:

Explanation:

- In **forward bias**, the ideal diode conducts **immediately at 0V**, allowing current to flow with **zero voltage drop**.
- In **reverse bias**, it blocks all current, acting like an **open switch**.

🔹 **Practical Diode Characteristics:**

A **practical diode** has a **threshold (cut-in) voltage** and allows **small reverse leakage current**.

Graphical Representation:

Explanation:

- In **forward bias**, a silicon diode begins to conduct after ~**0.7V** (cut-in voltage).
- In **reverse bias**, a small **leakage current** flows due to minority carriers until **breakdown** occurs at high voltage.

✅ **Summary Table:**

Property	Ideal Diode	Practical Diode
Forward Voltage Drop	0V	~0.7V (Si), ~0.3V (Ge)
Reverse Current	0 A	Small leakage current
Reverse Breakdown	Not applicable	Exists at high voltage

(b) Draw two-diode full-wave rectifier circuit and explain its operation. **04**

Answer:

Circuit Diagram:

Below is the circuit of a **Two-Diode Full-Wave Rectifier** using a center-tapped transformer:

Working Principle:

A **full-wave rectifier** converts the entire input AC waveform into a **pulsating DC output**. The operation is divided into two half-cycles:

➤ **Positive Half-Cycle:**

- The upper end of the transformer secondary is **positive**, and the lower end is **negative**.
- **Diode D1 conducts** (forward-biased), and **D2 is reverse-biased**.
- Current flows through **D1 → Load (RL) → Center tap**, producing a positive half-cycle across RL.

➤ **Negative Half-Cycle:**

- The polarity of the transformer secondary reverses.
- Now, **D2 conducts**, and **D1 is reverse-biased**.
- Current flows through **D2 → Load (RL) → Center tap**, again producing a **positive voltage** across RL.

🔹 **Conclusion:**

- In both half-cycles, **current through RL is in the same direction**, giving **full-wave rectification**.

(c) Explain positive and negative voltage clamper circuit with waveforms. **07**

Answer:

1. Introduction to Clamper Circuit:

A **clamper** is an electronic circuit that **adds or subtracts a DC level** to an AC signal **without changing its shape**. It shifts the **entire waveform** up or down vertically, so that either the **positive or negative peak** touches a defined reference voltage.

Clamper circuits use **a diode, a capacitor**, and sometimes a **DC source** and resistor.

✅ **2. Positive Clamper:**

🔹 **Definition:**

A **positive clamper** shifts the input waveform **upward**, so the **entire signal lies above the 0V (ground)** level. It **clamps the negative peak to zero** (or another reference).

🔹 **Circuit Diagram:**

🔹 **Working:**

- During the **negative half-cycle**, the diode conducts and capacitor charges.
- During the **positive half-cycle**, the diode becomes reverse-biased, and the capacitor adds its voltage to the input, pushing the waveform **upward**.

🔹 **Waveform:**

3. Negative Clamper:

🔹 **Definition:**

A **negative clamper** shifts the input waveform **downward**, so the **entire signal lies below the 0V level**. It **clamps the positive peak to zero**.

🔹 **Circuit Diagram:**

- Diode is reversed compared to the positive clamper.

🔹 **Working:**

- During the **positive half-cycle**, the diode conducts and capacitor

charges.

- During the **negative half-cycle**, the diode is reverse-biased, and the capacitor adds voltage to the signal, **shifting the waveform downward**.

🔹 **Waveform:**

4. Key Characteristics of Clamper Circuits:

- Maintains waveform shape
- Alters DC level
- Depends on capacitor charging
- Polarity of diode determines **positive or negative clamping**

✅ **5. Applications of Clamper Circuits:**

- Television receivers (DC restoration)
- Signal conditioning
- Oscilloscope input protection
- Wave shaping circuits

✅ **Conclusion:**

Clamper circuits are used to **shift the entire AC waveform up or down**, based on whether it is a **positive or negative clamper**. This is achieved using a **diode and capacitor**, and is useful in many analog and digital systems.

Q.2 (a) What are three modes of transistor operation, explain it. **03**

Answer:

Three Modes of Transistor Operation

A **bipolar junction transistor (BJT)** operates in **three different modes** depending on the biasing of the **emitter-base** and **collector-base** junctions:

---

1. Active Mode

- **Condition**:
  - **Emitter-Base Junction (EBJ)** → Forward Biased
  - **Collector-Base Junction (CBJ)** → Reverse Biased
- **Use**: Transistor acts as an **amplifier**.
- **Explanation**: In this mode, a small base current controls a large collector current.

---

2. Cut-off Mode

- **Condition**:
  - **EBJ** → Reverse Biased
  - **CBJ** → Reverse Biased
- **Use**: Transistor acts as an **OFF switch**.
- **Explanation**: Very little or no current flows; both junctions block current.

---

3. Saturation Mode

- **Condition**:
  - **EBJ** → Forward Biased
  - **CBJ** → Forward Biased
- **Use**: Transistor acts as an **ON switch**.
- **Explanation**: Maximum current flows through the transistor with

minimal voltage drop across it.

✅ **Summary Table:**

Mode	EB Junction Bias	CB Junction Bias	Application
Active	Forward	Reverse	Amplifier
Cut-off	Reverse	Reverse	OFF Switch
Saturation	Forward	Forward	ON Switch

(b) What is you understand by transistor biasing and why it is required. **04**

Answer:
Transistor Biasing – Definition:
Transistor biasing is the process of **applying external DC voltages and currents** to a transistor to establish a **desired operating point** (also known as the **Q-point** or **quiescent point**) for its proper functioning in amplifier or switching applications.

🔹 **Need for Transistor Biasing:**

1. **To establish correct Q-point:**
   Ensures that the transistor operates in the **active region**, which is necessary for **linear amplification**.
2. **To avoid distortion:**
   Without proper biasing, the output signal may get **clipped or distorted**.
3. **For thermal stability:**
   Proper biasing **compensates for temperature variations** that can affect transistor performance.
4. **To ensure consistent gain:**
   Biasing keeps **current and voltage levels steady**, allowing the amplifier to produce uniform gain.
5. **To prevent cutoff and saturation:**
   Biasing avoids the transistor slipping into **cutoff** (no conduction) or **saturation** (maximum conduction) unintentionally.

✅ **Conclusion:**
Transistor biasing is essential to make the transistor function **correctly and reliably** in analog circuits by setting a suitable Q-point and maintaining it during signal operation.

(c) Compare CB, CE and CC configuration. **07**

Answer:
1. Introduction:
A **bipolar junction transistor (BJT)** can be connected in three configurations based on the terminal common to both input and output:

- **CB** – Common Base
- **CE** – Common Emitter
- **CC** – Common Collector

Each configuration has **unique characteristics** in terms of gain,

impedance, and phase shift, and is used in different circuit applications.

✅ **2. Comparison Table of CB, CE, and CC Configurations:**

Parameter	Common Base (CB)	Common Emitter (CE)	Common Collector (CC)
Input Terminal	Emitter	Base	Base
Output Terminal	Collector	Collector	Emitter
Common Terminal	Base	Emitter	Collector
Input Impedance	Low	Medium	High
Output Impedance	High	High	Low
Current Gain (β or α)	< 1 (α ≈ 0.95–0.99)	High (20 to 500)	High (same as CE)
Voltage Gain	High	High	Less than 1
Power Gain	Medium	High	Medium
Phase Shift (Input-Output)	0° (no phase reversal)	180° (inverted)	0° (no phase reversal)
Application	High-frequency amplifiers	General-purpose amplifiers	Buffering, impedance matching
Signal Inversion	No	Yes	No

✅ **3. Graphical Representation:**

OR

(c) Explain the operation of voltage divider bias circuit using an npn transistor and write its voltage and current equation. **07**

Answer:

1. Introduction:

The **voltage divider bias** is the most widely used method to **bias a transistor** in the **active region**, ensuring **stable operation** regardless of transistor parameter variations. It uses a **voltage divider network** formed by two resistors to set the base voltage.

✅ **2. Circuit Diagram:**

(*You should draw this simple circuit in your exam*)

3. Operation of the Voltage Divider Bias:

1. **Base Voltage (VB):**
   The resistors R1 and R2 form a voltage divider from Vcc to ground:

$$V_B = \frac{R_2}{R_1 + R_2} \cdot V_{CC}$$

2. **Base Current (IB):**
   Using Kirchhoff's law in the base-emitter loop:

$$I_B = \frac{V_B - V_{BE}}{R_B + (\beta + 1)R_E}$$

(Simplified by Thevenin's equivalent method in analysis)

3. **Emitter Current (IE):**

$$I_E \approx \frac{V_B - V_{BE}}{R_E}$$

4. **Collector Current (IC):**
   Since IE ≈ IC (as IB is small),
   $$IC \approx IE$$
5. **Collector Voltage (VC):**
   $$VC = VCC - IC \cdot RC$$
6. **Collector-Emitter Voltage (VCE):**
   $$VCE = VC - IE \cdot RE$$

✅ **4. Key Features:**

- Provides **stable Q-point** (operating point)
- Minimizes effect of **β variation** (transistor parameter)
- Negative feedback through R_E improves thermal stability

✅ **5. Applications:**

- Used in **amplifier circuits**
- Used in **signal processing**
- Preferred in **analog circuit design** for **stability**

✅ **Conclusion:**

The **voltage divider bias circuit** is highly reliable and ensures **thermal and bias point stability** for transistor operation. It is preferred in practical electronic design for **predictable and consistent performance** of the transistor amplifier.

Q.3 **(a)** What is photo-diode and how it works? **03**

Answer:

A **photodiode** is a **light-sensitive semiconductor device** that converts **light energy into electrical current**. It operates in **reverse bias** and is specially designed to detect light (photons).

Working Principle:

- The photodiode is always operated in **reverse bias**.
- When **no light** falls on the photodiode, only a small leakage current (dark current) flows.
- When **light (photons)** strikes the junction, it generates **electron-hole pairs**.
- These charge carriers are swept across the junction by the electric field due to reverse bias, producing a **photocurrent**.
- The magnitude of this current is **directly proportional** to the intensity of incident light.

Symbol of Photodiode:

(b) What is varactor diode, and explain how it works? **04**

Answer:

What is a Varactor Diode?

A **Varactor Diode** (also called a **Varicap** or **Variable Reactance Diode**) is a **special-purpose semiconductor diode** that is **designed to act as a variable capacitor** when **reverse-biased**.

- It **does not conduct current** under normal reverse bias.
- It is used in **tuning circuits**, such as in radios, TV tuners, and communication devices.

🔹 **Working Principle of Varactor Diode:**

- When a **reverse voltage** is applied to a varactor diode, **no current flows**, but a **depletion layer** forms at the junction.
- This depletion layer acts as a **dielectric**, and the **P-N junction** acts like a **capacitor**.
- As the **reverse bias voltage increases**, the **depletion region widens**, and the **capacitance decreases**.
- Conversely, reducing the reverse voltage **increases the capacitance**.

□ Thus, the **capacitance is controlled by the applied reverse voltage**.

🔹 **Capacitance Formula:**

$$C_j = \frac{C_0}{\left(1 + \frac{V_R}{V_T}\right)^n}$$

Where:

- Cj = junction capacitance
- C0 = capacitance at zero bias
- VR = applied reverse voltage
- VT = threshold voltage
- n = constant depending on doping level

✅ **Conclusion:**

Varactor diodes are **widely used** in electronic circuits where **variable capacitance is required**, especially in **voltage-controlled oscillators**, **RF filters**, and **frequency modulators**.

(c) In CE amplifier has h_{ie} = 2.1 KΩ, h_{fe} = 75 and h_{oe} =1 µS, voltage divider resistance R_1= 68 kΩ and R_2= 56 kΩ, Rc=3.9 kΩ, R_E= 4.7 kΩ and R_L= 82 kΩ. Calculate input impedance, output impedance and voltage gain. **07**

Answer:

given:

- **hie** = 2.1 kΩ
- **hfe** = 75
- **hoe** = 1 µS
- **R_1** = 68 kΩ
- **R_2** = 56 kΩ
- **RC** = 3.9 kΩ
- **RE** = 4.7 kΩ
- **RL** = 82 kΩ

Calculate:

1. Input impedance (Zin)
2. Output impedance (Zout)
3. Voltage gain (Av)

✅ **1. Input Impedance (Zin):**

In a CE amplifier, the **input impedance (Zin)** is mainly determined by:

$$Z_{in} = R_1 \parallel R_2 \parallel h_{ie}$$

$$R_1 = 68\,k\Omega, \quad R_2 = 56\,k\Omega, \quad h_{ie} = 2.1\,k\Omega$$

First, calculate R1∥R2:

$$R_{12} = \frac{R_1 \cdot R_2}{R_1 + R_2} = \frac{68 \times 56}{68 + 56} = \frac{3808}{124} \approx 30.7\,k\Omega$$

Now, calculate Zin=R12∥hie:

$$Z_{in} = \frac{30.7 \times 2.1}{30.7 + 2.1} \approx \frac{64.47}{32.8} \approx 1.96\,k\Omega$$

✅ **Answer: Input Impedance Zin ≈ 1.96 kΩ**

✅ **2. Output Impedance (Zout):**

Output impedance is approximated using:

Zout=RC∥RL

$$R_C = 3.9\,k\Omega, \quad R_L = 82\,k\Omega$$

$$Z_{out} = \frac{3.9 \times 82}{3.9 + 82} = \frac{319.8}{85.9} \approx 3.72\,k\Omega$$

✅ **Answer: Output Impedance Zout ≈ 3.72 kΩ**

✅ **3. Voltage Gain (Av):**

Voltage gain of CE amplifier (neglecting RE in AC analysis if bypassed):

$$A_v = -\frac{h_{fe} \cdot R_{AC}}{h_{ie}}$$

Where:

$$R_{AC} = R_C \parallel R_L = 3.72\,k\Omega, \quad h_{fe} = 75, \quad h_{ie} = 2.1\,k\Omega$$

$$A_v = -\frac{75 \times 3.72}{2.1} \approx -\frac{279}{2.1} \approx -133$$

✅ **Answer: Voltage Gain Av ≈ –133**

✅ **Final Answers:**

Quantity	Value
Input Impedance Zin	≈ 1.96 kΩ
Output Impedance Zout	≈ 3.72 kΩ
Voltage Gain Av	≈ –133

OR

Q.3 (a) What is tunnel diode, and explain how it works? **03**

Answer:
A **tunnel diode** is a **heavily doped PN junction diode** that exhibits **negative resistance** in a certain region of its V-I characteristics. It is used mainly for **high-speed switching and microwave applications**.

Working Principle:

- In a tunnel diode, due to **heavy doping**, the **depletion layer is very narrow** (about 10^{-6} cm).
- When a **small forward voltage** is applied, electrons **tunnel** through the narrow junction from the conduction band of the N-side to the valence band of the P-side. This results in **tunneling current**.
- As the voltage increases further, tunneling decreases and the **current also decreases**, resulting in **negative resistance** region.
- Beyond this region, normal diode conduction takes place.

Key Characteristics:

- **Operates at very high frequency**.
- Exhibits **negative resistance** region in its V-I curve.
- Suitable for **oscillators and amplifiers** in microwave circuits.

Labelled Diagram (V-I Characteristics):

(b) Explain how Zener diode maintains constant voltage across load with circuit. **04**

Answer:
Zener Diode – Overview:
A **Zener diode** is a specially designed **reverse-biased diode** that maintains a **constant voltage** across the load even when the **input voltage or load current changes**. This voltage is called the **Zener breakdown voltage**.

🔹 **Zener Diode Voltage Regulator Circuit:**
Circuit Diagram:

Working Principle:

1. When the input voltage increases, the **Zener diode conducts** in **reverse breakdown** mode.
2. The **excess voltage** is **dropped across resistor R**, and **Zener voltage remains constant** across the load.
3. If input voltage drops **below the Zener voltage**, the diode **stops conducting**, and load voltage follows input.

🔹 **Why It Maintains Constant Voltage:**

- In **breakdown region**, the Zener diode keeps its voltage nearly **constant**.
- It compensates for fluctuations in the input by adjusting the **current through the series resistor (R)**, thus **protecting sensitive load circuits**.

✅ **Conclusion:**

Zener diode is **widely used** as a **voltage regulator** because it maintains a **fixed output voltage** across the load, making it essential in **power supplies** and **electronic protection circuits**.

(c) Draw single stage CE amplifier and analyze and explain how it works. **07**

Answer:
1. Introduction:
A **Single Stage Common Emitter (CE) Amplifier** is one of the most widely used transistor amplifier configurations. It is known for providing **high voltage gain**, **moderate current gain**, and **180° phase shift** between input and output signals.

✅ **2. Circuit Diagram:**

Components:
- **R1 & R2**: Voltage divider biasing resistors
- **Rc**: Collector resistor
- **Re**: Emitter resistor (for stability)
- **Cin**: Input coupling capacitor
- **Cout**: Output coupling capacitor
- **Ce**: Emitter bypass capacitor (for gain)

✅ **3. Working Principle:**

🔷 **Biasing:**
- The **voltage divider network** (R1 and R2) sets the **base voltage**.
- The **transistor is biased in active region**, ensuring proper amplification.

🔷 **Input Stage:**
- The input AC signal is applied via **Cin**, which **blocks DC** and passes only AC to the base.

🔷 **Amplification:**
- The small AC input signal modulates the **base current (IB)**, which gets **amplified** into a large **collector current (IC)** due to transistor action.
- This causes a large **voltage drop across Rc**, resulting in an amplified **output signal** at the collector.
- **Note:** Output is **180° out of phase** with the input.

🔷 **Output Stage:**
- The amplified AC output is taken via **Cout**, which blocks DC and allows only the amplified AC signal to pass.

🔷 **Stabilization:**
- **Re** provides **negative feedback**, stabilizing the gain and bias point.
- **Ce** (bypass capacitor) is used to **short Re** for AC signals to **maximize gain**.

✅ **4. Key Parameters:**
- **Voltage Gain (Av):**

$$A_v = -\frac{h_{fe} \cdot R_C}{h_{ie}}$$

(or approximated by small signal analysis)

- **Input Impedance (Zin):** Moderate
- **Output Impedance (Zout):** High
- **Phase Shift:** 180° between input and output

✅ **5. Applications:**
- Audio amplifiers
- Signal processing circuits
- Intermediate stages of multistage amplifiers

✅ **6. Conclusion:**
The **single-stage CE amplifier** is essential in electronics for its ability to **amplify small AC signals** with a **significant voltage gain**. Its **simple design**, **stability**, and **phase inversion** make it suitable for many analog applications.

Q.4 (a) Define saturation current, pinch off voltage and transconductance in JFET. **03**

Answer:
1. Saturation Current (IDSS):
It is the **maximum drain current** that flows through the JFET when the **gate-to-source voltage (VGS) is zero** and the **drain-to-source voltage (VDS) is sufficiently high** to make the channel saturated.
- It is denoted as **IDSS**.
- It occurs in the **saturation (or pinch-off) region**.
- It is the **maximum current** the JFET can conduct without any gate bias.

---

2. Pinch-off Voltage (VP):
Pinch-off voltage is the **drain-to-source voltage (VDS)** at which the **JFET enters the saturation region**, and the drain current becomes **constant (ID = IDSS)**.
- It is denoted as **VP** or **VGS(off)** (depending on context).
- For **VGS = 0**, once **VDS ≥ VP**, the current saturates.

---

3. Transconductance (gm):
Transconductance is the **rate of change of drain current (ID)** with respect to the **gate-to-source voltage (VGS)**, keeping **drain-to-source voltage (VDS) constant**.

$$g_m = \frac{dI_D}{dV_{GS}}$$

- It represents the **amplification capability** of the JFET.
- It is **analogous to gain** in bipolar junction transistors.

(b) Do comparison between BJT and FET and write it. **04**

Answer:
Comparison between BJT and FET:

Parameter	BJT (Bipolar Junction Transistor)	FET (Field Effect Transistor)
Type of Device	Current-controlled device	Voltage-controlled device

Input Impedance	Low	High
Control Element	Base current controls collector current	Gate voltage controls drain current
Noise Level	More noise	Less noise
Thermal Stability	Less	Better
Gain	Higher voltage gain	Lower voltage gain
Size and Construction	Larger, more complex	Smaller, simpler
Power Consumption	More	Less
Applications	Amplifiers, switches	Buffer, amplifiers, analog switches

---

✅ **Conclusion:**

- **BJT** is preferred where **high gain** is required.
- **FET** is used where **high input impedance**, **low power**, and **low noise** are needed.

(c) Analyze and explain CB amplifier and find its input impedance, output impedance and voltage gain **07**

Answer:

1. Introduction:

The **Common Base (CB) amplifier** is a BJT amplifier configuration where the **base terminal is common** to both input and output. The input signal is applied between the **emitter and base**, and the output is taken across the **collector and base**.

It is known for:

- **Low input impedance**
- **High output impedance**
- **High voltage gain**
- **No phase reversal** between input and output

✅ **2. CB Amplifier Circuit Diagram:**

3. Working of CB Amplifier:

1. **Biasing**: Proper DC biasing is done to operate the transistor in the **active region**.
2. **Signal Amplification**: A small input signal at the **emitter** controls a large current flowing through the **collector**.
3. The output voltage is developed across the **collector resistor (Rc)**.
4. There is **no phase inversion** — the output is **in phase** with the input.

✅ **4. Important Parameters:**

Let us assume:

- hie: Input resistance of transistor
- hfe: Current gain in CE
- α=hfe/1+hfe: Current gain in CB
- RC: Collector resistance

- RL: Load resistance
- re: Dynamic emitter resistance ≈ 25mV/IE

✅ **(i) Input Impedance (Zin):**

$$Z_{in} = r_e \approx \frac{25\,mV}{I_E}$$

- Very **low** input impedance (typically 30–100 Ω)
- Because input is applied to **forward-biased emitter-base junction**

✅ **(ii) Output Impedance (Zout):**

$$Z_{out} = R_C \parallel r_o$$

Where:

- RC = collector resistance
- ro = output resistance of transistor (typically high)

So, **Zout is high**, typically in **kΩ range**.

✅ **(iii) Voltage Gain (Av):**

$$A_v = \frac{V_{out}}{V_{in}} = \frac{\alpha \cdot R_C}{r_e}$$

- Since α≈0.98, voltage gain is **high**
- No phase reversal (0° phase shift)

✅ **5. Summary of Characteristics:**

Parameter	**Value/Behavior**
Input Impedance	Low (≈ 30–100 Ω)
Output Impedance	High (≈ kΩ)
Voltage Gain	High (typically 100–300)
Phase Shift	0° (no inversion)
Application	High-frequency amplifiers

✅ **6. Applications of CB Amplifier:**

- **Radio Frequency (RF) amplifiers**
- **Impedance matching** in communication circuits
- **Low-noise amplifiers**

✅ **Conclusion:**

The **CB amplifier** is ideal where **low input impedance and high voltage gain** are required. It is widely used in **RF applications** due to its stability at high frequencies.

OR

Q.4 **(a)** Define performance parameter of JFET a.c. drain resistance, transconductance and amplification factor. **03**

Answer:

1. A.C. Drain Resistance (rd):

A.C. drain resistance is the **small signal resistance** offered by the JFET in the **saturation region**, measured as the **change in drain-to-source voltage (ΔVDS)** divided by the **corresponding change in drain current (ΔID)**, keeping gate-to-source voltage (VGS) constant.

$$rd=(\Delta VDS/\Delta ID)\ VGS=constant$$

- It is typically **high** for a JFET.
- Measured in **ohms (Ω)**.

---

2. Transconductance (gm):

Transconductance is defined as the **rate of change of drain current (ID)** with respect to the **gate-to-source voltage (VGS)**, while keeping the **drain-to-source voltage (VDS) constant**.

$$gm=(\Delta ID/\Delta VGS)\ VDS=constant$$

- It indicates the **gain capability** of the JFET.
- Measured in **siemens (S)** or **mho**.

---

3. Amplification Factor (μ):

Amplification factor is the **product** of the transconductance (gm) and the A.C. drain resistance (rd).

$$\mu=gm \times rd$$

- It represents the **voltage gain capability** of the JFET.
- It is a **dimensionless quantity**.

(b) In n-channel JFET with $V_{GS(off)}$ =-6 V and I_{DSS} = 3 mA Solve I_D value for V_{GS} =-1,-3, and -5 V. **04**

Answer:

For an **n-channel JFET**, the **drain current** (I_D) is calculated using the **Shockley's equation**:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

Given:

- IDSS = 3 mA
- VGS(off) = –6 V

- **Case 1: V_{GS} = –1 V**

$$I_D = 3\left(1 - \frac{-1}{-6}\right)^2 = 3\left(1 - \frac{1}{6}\right)^2 = 3\left(\frac{5}{6}\right)^2$$

$$I_D = 3 \times \frac{25}{36} = \frac{75}{36} = 2.08\ \text{mA (approx)}$$

- **Case 2: V_{GS} = –3 V**

$$I_D = 3\left(1 - \frac{-3}{-6}\right)^2 = 3\left(1 - \frac{3}{6}\right)^2 = 3\left(\frac{3}{6}\right)^2$$

$$I_D = 3 \times \left(\frac{1}{2}\right)^2 = 3 \times \frac{1}{4} = 0.75\ \text{mA}$$

🔹 **Case 3: VGS = –5 V**

$$I_D = 3\left(1 - \frac{-5}{-6}\right)^2 = 3\left(1 - \frac{5}{6}\right)^2 = 3\left(\frac{1}{6}\right)^2$$

ID=3×1/36=3/36=0.083 mA (approx)

✅ **Final Answer Summary:**

VGS (V)	ID (mA)
–1	2.08
–3	0.75
–5	0.083

(c) Consider a CB amplifier utilizing a BJT biased at Ic= 1 mA with Rc = 5 kΩ, R_L= 5 kΩ. Determine Rin, Avo, Av, and Ro. **07**

Answer:

1. Given Data:

- **IC = 1 mA**
- **RC = 5 kΩ**
- **RL = 5 kΩ**
- Assume thermal voltage, **VT ≈ 25 mV**
- Common base amplifier, so:
  - Input at emitter
  - Output at collector
  - Base is grounded (AC-wise)

✅ **2. Input Resistance (Rin):**

In a CB amplifier, input resistance is very low and approximately:

$$R_{in} = r_e = \frac{V_T}{I_E} \approx \frac{25\ \text{mV}}{1\ \text{mA}} = 25\ \Omega$$

✅ **Answer:**

Rin=25 Ω

✅ **3. Open-Circuit Voltage Gain (Avo):**

$$A_{vo} = \frac{V_{out}}{V_{in}} = \frac{\alpha \cdot R_C}{r_e}$$

- Assume **α ≈ 1** (since α = β / (1 + β), and β is large)

$$A_{vo} = \frac{5\ \text{k}\Omega}{25\ \Omega} = 200$$

✅ **Answer:**

Avo=200

✅ **4. Loaded Voltage Gain (Av):**
When load is connected, effective collector resistance becomes:

$$R_{ac} = R_C \parallel R_L = \frac{5 \times 5}{5 + 5} = \frac{25}{10} = 2.5\ \text{k}\Omega$$

Then,

$$A_v = \frac{R_{ac}}{r_e} = \frac{2.5\ \text{k}\Omega}{25\ \Omega} = 100$$

✅ **Answer:**

Av=100

✅ **5. Output Resistance (Ro):**
For a CB amplifier, output resistance is approximately equal to:

Ro=RC=5 kΩ

(Since the transistor's internal output resistance r_o is very high and often neglected)

✅ **Answer:**

Ro=5 kΩ

✅ **Final Answer Summary:**

Parameter	**Value**
Input Resistance (Rin)	25 Ω
Open-Circuit Gain (Avo)	200
Loaded Gain (Av)	100
Output Resistance (Ro)	5 kΩ

Q.5 (a) What is logic gates and state the rule used for OR and AND gate. **03**

Answer:
Logic Gate:
A **logic gate** is a basic building block of a digital circuit. It performs a **logical operation** on one or more binary inputs and produces a single binary output.
Each input and output is represented using two logic levels:

- **Logic 1** → HIGH (usually +5V)
- **Logic 0** → LOW (usually 0V)

Rules for Logic Gates:

---

1. OR Gate Rule:

- The output of the OR gate is **HIGH (1)** if **any one** or **more inputs** are

HIGH.

- The output is **LOW (0)** only if **all inputs** are LOW.

Truth Table:

Input A	Input B	Output Y = A + B
0	0	0
0	1	1
1	0	1
1	1	1

---

2. AND Gate Rule:

- The output of the AND gate is **HIGH (1)** only if **all inputs** are HIGH.
- The output is **LOW (0)** if **any input** is LOW.

Truth Table:

Input A	Input B	Output Y = A · B
0	0	0
0	1	0
1	0	0
1	1	1

(b) Why NAND and NOR gates are called universal gate and draw truth table of NAND gate. **04**

Answer:

Why NAND and NOR are Called Universal Gates:

- **NAND** and **NOR** gates are called **universal gates** because **any logic gate** (AND, OR, NOT, XOR, etc.) can be constructed using only **NAND or NOR** gates.
- This makes them **versatile** and **cost-effective** for digital circuit design.
- For example:
  - **NOT gate** using NAND: Connect both inputs of NAND gate together.
  - **AND/OR gates** can be made using a combination of NAND/NOR gates.

Hence, they are termed as **universal building blocks** in digital electronics.

◆ **Truth Table of NAND Gate:**

A **NAND gate** gives an output **LOW (0)** only when **both inputs are HIGH (1)**.

Input A	Input B	Output (A·B)'
0	0	1
0	1	1
1	0	1
1	1	0

✅ **Conclusion:**

- NAND and NOR gates are essential in digital logic design.
- Their ability to form all other logic gates makes them **universal gates**, and thus widely used in **integrated circuits** and **microprocessors**.

(c) Write and explain application of FET as amplifier and as a switch. **07**

Answer:

1. Introduction to FET:

A **Field Effect Transistor (FET)** is a voltage-controlled semiconductor device where the output current is controlled by the input voltage applied at the **gate terminal**. FETs are widely used due to their **high input impedance**, **low noise**, and **low power consumption**.

✅ **2. FET as an Amplifier:**

🔷 **Working Principle (Amplifier Mode):**

In amplifier applications, the **FET is operated in the saturation (or active) region**, where:

- **Gate-Source voltage (VGS)** controls the **drain current (ID)**.
- A small **AC signal at the gate** causes a **large variation in the drain current**, which results in an amplified voltage across the drain resistor (RD).

🔷 **Circuit Diagram (Common Source Amplifier):**

Key Features:

- **Voltage Amplification** is achieved.
- **High input impedance** avoids loading of the previous stage.
- **No gate current flows**, so power consumption is low.

🔷 **Applications:**

- **Audio amplifiers**
- **RF amplifiers**
- **Buffer amplifiers**
- **Oscillator circuits**

✅ **3. FET as a Switch:**

🔷 **Working Principle (Switching Mode):**

The FET operates as a **digital switch** between ON and OFF states:

- **ON State (Switch Closed):**
  When VGS is sufficiently negative (for p-channel) or positive (for n-channel), the FET conducts (channel is formed), allowing current to flow.
- **OFF State (Switch Open):**
  When VGS is 0 or below threshold, the channel is pinched off, and the FET does not conduct.

🔷 **Switching Circuit Diagram (n-channel MOSFET example):**

Key Features:

- **Fast switching speed**

- **Low ON resistance**
- **High OFF resistance (ideal open circuit)**
- **No gate current** needed — ideal for digital circuits

🔷 **Applications:**
- **Digital logic circuits**
- **Analog signal switching**
- **Relay replacement**
- **Microcontroller interface circuits**

✅ **4. Conclusion:**
FETs are **versatile semiconductor devices**. As **amplifiers**, they are used in analog applications due to **high gain and input impedance**. As **switches**, they are essential in digital and power electronics because of **fast, efficient operation** with minimal power loss.

OR

Q.5 **(a)** Draw the logic circuit for the Boolean expression Y = ABC + $\bar{D}$. **03**

Answer:
Given Boolean Expression:

$$Y=A\cdot B\cdot C+\bar{D}$$

This expression involves:
- **AND operation** between A, B, and C
- **NOT operation** on D
- **OR operation** between the two parts: (ABC) and ($\bar{D}$)

---

1. Logic Circuit Diagram:

2. Explanation:
- First, connect inputs A, B, and C to a **3-input AND gate** to obtain the term **ABC**.
- Then, pass input **D** through a **NOT gate** to obtain $\bar{\mathbf{D}}$.
- Finally, connect the outputs of both the AND gate (ABC) and the NOT gate ($\bar{D}$) to an **OR gate** to get the final output:

$$Y=ABC+\bar{D}$$

(b) Explain Transistor Transistor Logic (TTL). **04**

Answer:
Transistor-Transistor Logic (TTL):
- **TTL** stands for **Transistor-Transistor Logic**.
- It is a **digital logic family** built entirely using **bipolar junction transistors (BJTs)**.
- TTL circuits perform **logic operations** such as AND, OR, NOT using transistors.

🔹 **Features of TTL:**
1. **Logic Levels:**
   - Logic **'0'** = 0 to 0.8 V
   - Logic **'1'** = 2 to 5 V
2. **Speed:**
   - TTL offers **moderate to high-speed operation**, typically in

the range of **10 ns to 30 ns**.

3. **Power Consumption:**
   - TTL consumes more power than CMOS but less than earlier logic families.
4. **Fan-out:**
   - A typical TTL gate can drive **up to 10 other TTL inputs** (fan-out = 10).
5. **Standard IC Series:**
   - The standard TTL IC family includes **74XX** series (e.g., 7400 for NAND gate).

🔹 **Basic TTL NAND Gate (Using Transistors):**

- The simplest TTL circuit is the **NAND gate**, which uses **multi-emitter transistors** at the input and additional transistors for amplification and inversion.

🔹 **Applications:**

- TTL is used in:
  - Microprocessors
  - Digital clocks
  - Calculators
  - Simple computing devices

✅ **Conclusion:**

TTL is one of the most widely used and reliable **logic families** for digital circuit design, known for its **robustness**, **availability**, and **speed**.

(c) Using common source circuit have a R_1=5.6 MΩ, R_2= 1 MΩ, R_D=R_S = 2.7 KΩ, rd = 100 KΩ and Y_{fs} = 3000 µS calculate input impedance, output impedance and voltage gain. **07**

Answer:

1. Input Impedance Zin:

In FETs, the **input is applied to the gate**, which draws **no current**. Therefore, the input impedance is the **parallel combination** of gate biasing resistors R1 and R2:

$$Z_{in} = R_1 \parallel R_2 = \frac{R_1 \cdot R_2}{R_1 + R_2}$$

$$Z_{in} = \frac{5.6\,M\Omega \times 1\,M\Omega}{5.6\,M\Omega + 1\,M\Omega} = \frac{5.6}{6.6}\,M\Omega \approx 0.848\,M\Omega$$

✅ **Answer: Input Impedance Zin≈848 kΩ**

✅ **2. Output Impedance Zout:**

The **output impedance** of a common source FET amplifier is:

$$Z_{out} = R_D \parallel r_d$$

$$Z_{out} = \frac{2.7\,k\Omega \cdot 100\,k\Omega}{2.7\,k\Omega + 100\,k\Omega} \approx \frac{270000}{102.7} \approx 2.63\,k\Omega$$

✅ **Answer: Output Impedance Zout≈2.63 kΩ**

✅ **3. Voltage Gain Av:**

Voltage gain of a Common Source amplifier (neglecting source resistance if bypassed):

$$Av = -gm \cdot (RD \parallel rd)$$

Where gm=Yfs=3 mS

Already calculated:

$$R_D \parallel r_d = 2.63\,k\Omega = 2630\,\Omega$$

$$A_v = -3\,mS \cdot 2630 = -3 \times 10^{-3} \times 2630 = -7.89$$

✅ **Answer: Voltage Gain Av≈−7.89**

(The negative sign indicates 180° phase shift)

✅ **Final Answers Summary:**

Parameter	Value
Input Impedance Zin	≈ 848 kΩ
Output Impedance Zout	≈ 2.63 kΩ
Voltage Gain Av	≈ –7.89

****