

**GUJARAT TECHNOLOGICAL UNIVERSITY****BE - SEMESTER-III (NEW) EXAMINATION – SUMMER 2024****Subject Code:3130907****Date:29-06-2024****Subject Name: Analog & Digital Electronics****Time:10:30 AM TO 01:00 PM****Total Marks:70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.
4. Simple and non-programmable scientific calculators are allowed.

		Marks
<b>Q.1</b>	(a) List all ideal characteristics of an Op-Amp.	<b>03</b>
	(b) Classify the types of negative feedback and explain each in brief.	<b>04</b>
	(c) Draw and explain block diagram of a typical OP-AMP	<b>07</b>
<b>Q.2</b>	(a) Compare the inverting and non-inverting comparators	<b>03</b>
	(b) Explain how to generate triangular wave using OPAMP	<b>04</b>
	(c) Draw the circuit Op-Amp as a Integrator and explain with necessary waveforms	<b>07</b>
	<b>OR</b>	
	(c) Explain positive peak detector circuit using OPAMP.	<b>07</b>
<b>Q.3</b>	(a) Calculate maximum frequency for a sine wave, output voltage of 12 V peak with an OPAMP having slew rate 1 V/ $\mu$ S	<b>03</b>
	(b) Explain the use of external offset voltage compensation circuits in op amps.	<b>04</b>
	(c) Explain the working of J- K flip flop with the help of diagram	<b>07</b>
	<b>OR</b>	
<b>Q.3</b>	(a) Reduce the following function using Boolean Algebra's Laws and Theorems $F=AB'C + B + BD' + ABD' + A'C$	<b>03</b>
	(b) Explain the operation of Zero crossing detector.	<b>04</b>
	(c) Describe 3 to 8 line decoder with logic diagram and truth table.	<b>07</b>
<b>Q.4</b>	(a) Compare decoder and demultiplexer.	<b>03</b>
	(b) Draw and Explain 4-bit bidirectional Shift Register.	<b>04</b>
	(c) Implement a full adder using 8 : 1 multiplexer.	<b>07</b>
	<b>OR</b>	
<b>Q.4</b>	(a) Differentiate the Asynchronous counter and Synchronous counter	<b>03</b>
	(b) Simply the following function using K map and implement using logic gates. $F = \sum m(2,9,10,12,13) + D(15,14)$	<b>04</b>
	(c) Explain full subtractor and construct full subtractor using half subtractors.	<b>07</b>
<b>Q.5</b>	(a) Define following specification of ADC i) Resolution ii) Conversion time and iii) Quantization error	<b>03</b>
	(b) Explain R-2R ladder DAC with necessary diagram	<b>04</b>
	(c) Describe operation of D/A converter with binary – weighted resistors	<b>07</b>
	<b>OR</b>	
<b>Q.5</b>	(a) Explain terms Accuracy and settling time for DAC	<b>03</b>
	(b) What will be resolution of 4 bit ADC with 5V input? Define quantization error for ADC.	<b>04</b>
	(c) Explain working of successive approximation type ADC	<b>07</b>

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