Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER– III EXAMINATION – SUMMER 2026

Subject Code:BE03000181 Date:24-06-2026

Subject Name:Digital System Design

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Define: Propagation Delay, fan-out, Noise Margin	**03**
	(b)	Convert (975)11 to decimal, binary, octal and hexadecimal number.	**04**
	(c)	Design a BCD to Excess-3 code converter.	**07**
Q.2	**(a)**	Draw a 3-input EX-OR gate write its truth table and derive its input-output relationship.	**03**
	(b)	State and prove De Morgan's theorems.	**04**
	(c)	Design a 4-bit binary adder cum subtractor.	**07**
		OR	
	(c)	Design and implement 4-bit binary magnitude comparator.	**07**
Q.3	**(a)**	Define: Resolution, Accuracy, Conversion time.	**03**
	(b)	Implement a full-addder with smallest size Multiplexer	**04**
	(c)	simplify the following Boolean function using K-map: P(A,B,C,D,E,F)=Σm(20,28,52,60) and implement using minimum number of logic gates	**07**
		OR	
Q.3	**(a)**	Define: Tri-state logic, Maxterm, Minterm	**03**
	(b)	Implement 2-input EX-OR function by only NAND gates.	**04**
	(c)	simplify the following Boolean function using tabulation: P(A,B,C,D,E,F)=Σm(20,28,52,60) and implement using minimum number of NOR gates.	**07**
Q.4	**(a)**	State the differences between PAL and PLA.	**03**
	(b)	Convert a JK FF to D-FF.	**04**
	(c)	Design a 3-bit binary synchronous up-counter with JK FF.	**07**
		OR	
Q.4	**(a)**	State the differences between ROM and PROM	**03**
	(b)	Convert an SR FF to D-FF.	**04**
	(c)	Design a 3-bit binary ripple counter using T-FF.	**07**
Q.5	**(a)**	Show CMOS implantation of F=A.(B+C)	**03**
	(b)	Implement a full-adder using PROM	**04**
	(c)	A 4-bit weighted resistor DAC has resistor value of 32 KΩ corresponding to LSB. Determine the Value of other resisters. Input voltage is 5 V. Feedback resistor is 3.2 KΩ. Determine the Value of other resisters Determine the output voltage corresponding to LSB. Also calculate full scale output.	**07**

OR

Q.5	**(a)**	Show CMOS implantation of F=A+(B.C)	**03**
	(b)	Implement a full-adder using PLA	**04**
	(c)	A 4-bit successive Approximation register based ADC has an input of 5.2 V. Show the complete state diagram to reach the final binary output. If 1 MHz clock is used, calculate the time required for the output to settle.	**07**

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