

GUJARAT TECHNOLOGICAL UNIVERSITY

BACHELOR OF ENGINEERING – SEMESTER 5 – EXAMINATION – SUMMER 2026

Subject Code: 3151105

Date: 30/05/2026

Subject Name: VLSI Design

Time: 02:30 PM TO 05:00 PM

Total Marks: 70

Instructions:

- 1. Attempt all questions.**
- 2. Make suitable assumptions wherever necessary.**
- 3. Figures to the right indicate full marks.**
- 4. Simple and non-programmable scientific calculators are allowed.**

- Q.1**
- (a) Draw VLSI Design Flow y chart and flow chart. **03**
 - (b) Define Regularity, Modularity and Locality **04**
 - (c) Derive threshold voltage equation of MOSFET **07**
- Q.2**
- (a) Compare Full custom, Semi-custom and Fully Programmable VLSI design style. **03**
 - (b) Compare Constant field and constant voltage Scaling techniques of MOSFET. **04**
 - (c) Explain Fabrication of n-MOSFET with neat sketch. **07**
- OR
- Q.2**
- (c) Derive drain current using gradual channel approximate **07**
- Q.3**
- (a) Draw VTC of practical Inverter and define all critical voltages **03**
 - (b) Draw resistive load inverter and Derive V_{IH} critical voltage equation of it. **04**
 - (c) Consider a resistive-load inverter circuit with $V_{DD}=5V$, $k_n'= 20 \mu A/V^2$, $V_{T0}= 0.8 V$, $R_L = 200 k\Omega$, and $W/L = 2$. Find noise margin high MN_H . **07**
- OR
- Q.3**
- (a) What is need of Design of Testability and Define Controllability and observability **03**
 - (b) Draw CMOS inverter and Derive V_{IL} critical voltage equation of it. **04**
 - (c) Consider a CMOS inverter with the following parameters: $V_{Ton} = 0.6 V$, $V_{Top} = - 0.7 V$, $K_n = 200 \mu A/V^2$, $K_p = 80 \mu A/V^2$ and $V_{DD} = 3.3 V$. Find noise margin low NM_L . **07**
- Q.4**
- (a) Draw three stage ring oscillator circuit and derive it generated signal frequency equation **03**
 - (b) Realize the following Boolean function using Transmission Gate: $F=AB+A'C'+AB'C$ **04**
 - (c) Draw i/p and o/p waveform during high to low transition of o/p for CMOS inverter and derive expression for ζ_{pHL} . Using differential equation method **07**
- OR
- Q.4**
- (a) Draw the circuit diagram of domino CMOS logic gate **03**
 - (b) Draw CMOS implementation of D latch with two inverters and two CMOS TG gates. **04**
 - (c) Derive switching power dissipation equation of CMOS inverter with idea step input. **07**

- Q.5** (a) Compare FinFET and Planar MOSFET **03**
- (b) What is the need of voltage bootstrapping? Draw voltage bootstrapping circuit. **04**
- (c) What is clock skew. Draw and Explain on chip clock generation and distribution circuits. **07**

OR

- Q.5** (a) Implement clocked JK latch using CMOS inverter. **03**
- (b) Explain latch up problem in CMOS inverter. Mention causes and remedy for avoiding latch up. **04**
- (c) Write a short note on Built In Self Test(BIST). **07**
