Seat No./Enrollment No.: _____

GUJARAT TECHNOLOGICAL UNIVERSITY
BACHELOR OF ENGINEERING – SEMESTER 7 – EXAMINATION – SUMMER 2026

Subject Code: 3171111 **Date: 20/05/2026**

Subject Name: Testing and Verification

Time: 02:30 PM TO 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

Q.1	**(a)**	Define following: 1.fault coverage 2.yield 3. fault detection efficiency.	**03**
	(b)	Explain the difference between testing and verification in the VLSI life cycle.	**04**
	(c)	What is the use of bridging fault models in VLSI Testing?List down and explain various bridging fault models.	**07**
Q.2	**(a)**	Differentiate between Ad hoc DFT techniques and Structured DFT.	**03**
	(b)	What are the different levels of abstraction in VLSI testing?Explain if brief.	**04**
	(c)	What is mean by scan design rules? Prepare a table showing design style, its scan design rule and recommended solution for it.	**07**
		OR	
Q.2	**(c)**	Demonstrate how a set of three D flip-flops can be converted into a scan chain using Muxed D design.	**07**
Q.3	**(a)**	Draw and explain RTL testability repair design flow.	**03**
	(b)	Compare: Fault simulation and Logic simulation	**04**
	(c)	Explain the purpose of scan configuration in scan synthesis with suitable examples.	**07**
		OR	
Q.3	**(a)**	Define Static Hazard.List and explain different types of it.	**03**
	(b)	How the signaling will be provided in scan chain in which a negative edge scan cell is followed by a positive scan cell?	**04**
	(c)	Give comparison of fault simulation techniques.	**07**
Q.4	**(a)**	Draw and explain clocked scan cell design with the help necessary waveforms.	**03**
	(b)	What are the advantages of parallel fault simulation? Name the different approaches of it	**04**
	(c)	What is event driven simulation? Explain zero-event driven simulation with the help of example. Draw necessary flow chart for the same.	**07**
		OR	
Q.4	**(a)**	Discuss wire delay.	**03**
	(b)	What is reconvergence model in verification?	**04**

	(c)	What is ternary logic? Write down basic operations for ternary logic for AND, OR and NOT gate.	**07**
Q.5	**(a)**	Write down different approaches of functional verification and define all.	**03**
	(b)	What is a verification plan? List down its components.	**04**
	(c)	What is the role of code coverage in verification? Explain it in detail.	**07**

OR

Q.5	**(a)**	System Verilog is preferred over other hardware verification languages to implement Test Benches in industry. Why?	**03**
	(b)	What is the use of linting tools ?What are the limitations of it ?	**04**
	(c)	Design 1x4 demultiplexer and write its testbench in any hardware description language (HDL)	**07**

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