Seat No./Enrollment No.: _____

GUJARAT TECHNOLOGICAL UNIVERSITY
BACHELOR OF ENGINEERING – SEMESTER 3 – EXAMINATION – SUMMER 2026

Subject Code: 3130704 **Date: 02/07/2026**

Subject Name: Digital Fundamentals

Time: 02:30 PM TO 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

Q.1	**(a)**	Convert the decimal number 163 to its equivalent binary, octal and hexadecimal forms.	**03**
	(b)	Convert the BCD number 10010111 into its equivalent decimal and Excess-3 code.	**04**
	(c)	What do you mean by universal gates, and which gates are universal? Convert NAND gate to OR gate. Convert NOR gate to AND gate.	**07**
Q.2	**(a)**	Define : priority encoder, SOP and POS	**03**
	(b)	Analyze the conditions for a 'Don't Care' term in K-map simplification and simplify the expression $F(W,X,Y,Z)=\sum m(1,3,7,11,15)$ with Don't Care $d(W,X,Y,Z)=\sum d(0,2,5)$.	**04**
	(c)	Design a full subtractor circuit using basic logic gates. Also write its truth table.	**07**
		OR	
Q.2	**(c)**	Implement a 4×16 decoder using two 3×8 decoders.	**07**
Q.3	**(a)**	Distinguish between synchronous and asynchronous (ripple) counters based on their clocking mechanism.	**03**
	(b)	Define the term : 'state table' for a sequential circuit, ripple counter	**04**
	(c)	Draw a neat diagram of a 4-bit right shift register and explain its operation	**07**
		OR	
Q.3	**(a)**	Analyze the state transition diagram for a Johnson (twisted ring) counter and explain its counting sequence for 4 flip-flops.	**03**
	(b)	Define the term 'ring counter' and briefly explain how it differs from a Johnson counter.	**04**
	(c)	Explain J-K flip-flop and T flip-flop along with diagram and excitation table.	**07**
Q.4	**(a)**	Compare the weighted resistor D/A converter with the R-2R ladder D/A converter based on complexity, accuracy and ease of expansion.	**03**
	(b)	Define the term 'Quantization' and 'Encoding' in the context of A/D conversion.	**04**
	(c)	Evaluate the advantages and disadvantages of the dual slope A/D converter compared to the Successive Approximation A/D converter	**07**
		OR	
Q.4	**(a)**	Describe the operation of a Successive Approximation A/D (SAR) converter and state its main specification regarding conversion time.	**03**
	(b)	List the main components of an Analog-to-Digital conversion process	**04**
	(c)	Justify the use of an R-2R ladder network over a weighted resistor network for high-resolution D/A converters. Evaluate the advantages and disadvantages of the both.	**07**
Q.5	**(a)**	Define Read Only Memory (ROM) and list its different types.	**03**

	(b)	Describe the architecture and use of Field Programmable Gate Arrays (FPGAs).	**04**
	(c)	Design a simple combinational logic function $F(A,B,C)=\sum m(0,1,2,5,7)$ and implement it using a Programmable Logic Array (PLA), clearly showing the internal connections.	**07**

OR

Q.5	**(a)**	Differentiate between static RAM (SRAM) and dynamic RAM (DRAM).	**03**
	(b)	Describe the concept of memory organization in semiconductor memories	**04**
	(c)	Implement the logic function $F(X,Y,Z)=\sum m(1,2,4,7)$ using a ROM as a PLD, showing the memory organization.	**07**

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GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III EXAMINATION – SUMMER 2025

Subject Code:3130704 Date:06-06-2025

Subject Name:Digital Fundamentals

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	State and Apply DeMorgan's theorem.: [(x+y)'+(x+y)']'=x+y	**03**
	(b)	Do As Directed: 1. Convert $(0.6875)_{10}$ to Binary. 2. Give the octal equivalent of hexadecimal numbers of DC.BA. 3. Convert $(101101.1101)_2$ to Hexadecimal. 4. Give the Truth Table of XOR gate.	**04**
	(c)	Prove that NAND and NOR gates are universal gates.	**07**
Q.2	**(a)**	Determine the value of base x if $(211)_x = (152)_8$	**03**
	(b)	Subtract $(111001)_2$ from $(101011)_2$ using 1's complement	**04**
	(c)	Simplify and implementation the following SOP function using NOR gates F(A,B,C,D)= ∑m(0,1,4,5,10,11,14,15)	**07**
		OR	
	(c)	Simplify the Boolean expression using K-map and implement using NAND gates F(A,B,C,D) = ∑m(0,2,3,8,10,11,12,14)	**07**
Q.3	**(a)**	Design the combinational circuit of 4 Bit Parallel Adder.	**03**
	(b)	Implement the following Boolean function using 8:1 multiplexer: F(A, B, C, D) = A'BD' + ACD + A'C' D +B'CD	**04**
	(c)	Design a combinational circuit with four input lines that represent a decimal digit in BCD and four output lines that generate the 9's complement of the input digit.	**07**
		OR	
Q.3	**(a)**	Design Truth table for the Half adder and write the expression for the sum and carry.	**03**
	(b)	Implement the following Boolean function using 8:1 multiplexer: F(A,B,C,D) = Σm (0,3,4,7,8,9,13,14)	**04**
	(c)	Design 5 to 32 line decoder using 3 to 8 line decoder and 2 to 4 line decoder.	**07**
Q.4	**(a)**	Explain about Ring counter.	**03**
	(b)	Describe how T flip-flop is converted into D flip-flop.	**04**
	(c)	What is the function of shift register? With the help of simple diagram explain its working.	**07**
		OR	
Q.4	**(a)**	Explain various applications of the register.	**03**
	(b)	Describe how JK flip-flop is converted into D flip-flop.	**04**
	(c)	Draw the state diagram of BCD ripple counter, develop its logic diagram and explain its operation.	**07**

Q.5	**(a)**	Write difference between PROM, PLA & PAL.	**03**
	(b)	Using 8x4 ROM, realize the expressions W(A,B,C) =∑m(0,1,3,5,7) ,X(A,B,C) =∑m(0,2,4,5) , Y(A,B,C) =∑m(1,2,4,7) , Z(A,B,C=∑m(0,3,5,6,7). Show the data at address 2 & 6.	**04**
	(c)	Implement the following function using PLA F1= ∑m(0,2,5,8,9,11),F2=∑m(1,3,8,10,13,15),F3=∑m(0,1,5,7,9,12,14).	**07**

OR

Q.5	**(a)**	Discuss : Field Programmable Gate Array (FPGA)	**03**
	(b)	Explain Successive Approximation type A/D converter.	**04**
	(c)	Give a brief on various types of memories.	**07**

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GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III (NEW) EXAMINATION – SUMMER 2024

Subject Code:3130704 Date:06-07-2024

Subject Name: Digital Fundamentals

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	List out various logic families. Also list characteristics of digital IC.	**03**
	(b)	State and prove De-Morgan's theorems using truth-tables.	**04**
	(c)	Implement AND, OR, EX-OR gates using NAND & NOR gates.	**07**
Q.2	**(a)**	Reduce the expression F = x'y'z +yz+ xz	**03**
	(b)	Convert the decimal Number 330.5 to base 4 and base 8.	**04**
	(c)	Design a Combinational circuit that convert Binary to BCD code converter.	**07**
		OR	
	(c)	Design a Combinational circuit that convert BCD to Excess 3 code converter.	**07**
Q.3	**(a)**	Minimize following Boolean function using K-map: Y(A,B,C,D) = Σ m(0, 1, 3, 5,6, 7, 10, 13,14, 15)	**03**
	(b)	Explain 4 – bit parallel adder with diagram.	**04**
	(c)	Design 2 - Bit Magnitude Comparator.	**07**
		OR	
Q.3	**(a)**	Design D FF using SR FF. Write truth table of D FF.	**03**
	(b)	Minimize following Boolean function using K-map: F(A,B,C,D) = Σ m(1, 5, 6, 12, 13, 14) + d(2, 4)	**04**
	(c)	Design 3-bit even parity generator circuit.	**07**
Q.4	**(a)**	Compare static RAM and dynamic RAM.	**03**
	(b)	Explain JK flip flop with its characteristic table and excitation table.	**04**
	(c)	Write a brief note on race around condition and its solution. Draw & explain the logic diagram of master-slave JK flip-flop.	**07**
		OR	
Q.4	**(a)**	Explain the types of ROM.	**03**
	(b)	Explain Look-ahead Carry generator	**04**
	(c)	Design a Synchronous counter with the following binary sequence: 0, 1, 3, 4,5, 7 and repeat. Use T – flip-flops	**07**
Q.5	**(a)**	Explain the working of a Counter.	**03**
	(b)	Explain R-2R ladder type D/A converter	**04**
	(c)	A combinational circuit is defined by the function F1 (A, B, C,) = Σ m (0,1,3,4) F2 (A, B, C,) = Σ m (1.2.3,4,5) Implement the circuit with a PLA having 3 inputs, 3 product term & 2 outputs.	**07**
		OR	
Q.5	**(a)**	Explain the working of SISO shift register.	**03**
	(b)	Explain the specification of D/A converter	**04**
	(c)	Describe operation of D/A converter with binary-weighted resisters	**07**

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Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III(NEW) EXAMINATION – SUMMER 2023

Subject Code:3130704 Date:01-08-2023

Subject Name:Digital Fundamentals

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Define the logic family properties: (i) fan in (ii) propagation delay (iii) power dissipation	**03**
	(b)	Convert the following number to the given base: (i) $(62)_{10} = (?)_2 = (?)_8$ (ii) $(AFB)_{16} = (?)_2 = (?)_8$	**04**
	(c)	Why NAND and NOR gates are called universal gates? Explain with appropriate example.	**07**
Q.2	**(a)**	Explain the half subtractor with logic circuit.	**03**
	(b)	Minimized the boolean expression using K-map $f(A, B, C, D) = \sum m\,(0, 1, 5, 6, 7, 8, 9) + d(10, 11, 12, 13, 14, 15)$	**04**
	(c)	Design BCD to excess-3 converter.	**07**
		OR	
	(c)	Design a circuit which compare two binary number whether $A>B$, $A=B$ or $A<B$.	**07**
Q.3	**(a)**	Draw the circuit of a J-K flip-flop.	**03**
	(b)	Describe the operation of a shift register with suitable diagram.	**04**
	(c)	Design the four bit Johnson counter and explain the operation.	**07**
		OR	
Q.3	**(a)**	Explain different methods of Triggering of flip-flop.	**03**
	(b)	What are qualitative differences between parallel loading and serial loading in shift registers?	**04**
	(c)	Design a 3 bit synchronous counter using JK flip flop.	**07**
Q.4	**(a)**	How can we describe the resolution of a D/A converter?	**03**
	(b)	A 10-bit D/A converter provides an analog output which has a maximum value of 10.23 volts. Find the resolution of this D/A converter.	**04**
	(c)	Explain the working of R-2R ladder type D/A converter.	**07**
		OR	
Q.4	**(a)**	Explain the types of A/D convertors.	**03**
	(b)	A 10-bit D/A converter has a step-size of 10 mV. Determine the full-scale output voltage and the percentage resolution.	**04**

(c) Describe the successive approximation A/D conversion principle with the neat diagram, explain this type of A/D converter. **07**

Q.5 **(a)** Draw and explain the structure of a RAM cell. **03**

(b) Implement using PLA **04**

$f_1 = \sum m(0, 3, 4, 7)$

$f_2 = \sum m(3, 5, 6, 7)$

(c) Discuss in brief semiconductor memory organization and its operation. **07**

OR

Q.5 **(a)** Compare the SRAMs and DRAMs. **03**

(b) Implement the following Boolean expressions using a PROM. **04**

$f_1 (x_2, x_1, x_0) = \Sigma\, m\, (0, 1, 2, 5, 7)$

$f_2 (x_2, x_1, x_0) = \Sigma\, m\, (1, 2, 4, 6)$

(c) What is a programmable LOGIC Array (PLA)? Describe with a logic diagram the principle of operation of a PLA. What are its advantages? **07**

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Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER– III (NEW) EXAMINATION – SUMMER 2022

Subject Code:3130704 Date:18-07-2022

Subject Name:Digital Fundamentals

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	List out various logic families. Also list characteristics of digital IC.	**03**
	(b)	What is signal? Explain different types of signal.	**04**
	(c)	Implement the following Boolean function using MUX a) $F(A,B,C) = \sum(1,3,6)$ b) $F(A,B,C) = \pi(2,3,5)$	**07**
Q.2	**(a)**	Perform the binary subtraction using 2's complement $(0111)_2 - (1101)_2$	**03**
	(b)	Convert the decimal Number 250.5 to base 4 and base 8.	**04**
	(c)	Design a Combinational circuit that convert 8- 4 -2 -1 code to BCD	**07**
		OR	
	(c)	Explain various logic gates.	**07**
Q.3	**(a)**	Compare Half adder and Full adder.	**03**
	(b)	Explain NAND gate as a Universal Gate.	**04**
	(c)	Implement 2-bit Magnitude comparator.	**07**
		OR	
Q.3	**(a)**	Simplify Boolean function using K-MAP F(A, B, C, D)=ABC'D' + ABC'D + ABCD' + AB'CD'	**03**
	(b)	Explain 4 bit Binary Parallel Adder.	**04**
	(c)	Explain Minterm and Maxterm.	**07**
Q.4	**(a)**	Give the difference between sequential circuit and combinational circuit.	**03**
	(b)	Explain Look-ahead Carry generator.	**04**
	(c)	Explain JK Flip-Flop.	**07**
		OR	
Q.4	**(a)**	Explain NAND SR Latch.	**03**
	(b)	Explain clock triggering mechanism.	**04**
	(c)	What is race around condition (racing)? How to solve it?	**07**
Q.5	**(a)**	Classify different types of digital to analog converters.	**03**
	(b)	Compare static RAM and dynamic RAM.	**04**
	(c)	List out different types of ROM. Also explain ROM.	**07**
		OR	
Q.5	**(a)**	Discuss the application of shift registers.	**03**
	(b)	Explain working of counter.	**04**
	(c)	Describe operation of D/A converter with binary-weighted resisters.	**07**

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