Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER–III EXAMINATION – WINTER 2025

Subject Code:3130704 Date:22-12-2025

Subject Name: Digital Fundamentals

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	List out various logic families. Also list characteristics of digital IC.	**03**
	(b)	Convert the decimal number 225.225 to octal and hexadecimal.	**04**
	(c)	Implement AND, OR, EX-OR gates using NAND & NOR gates.	**07**
Q.2	**(a)**	Draw the logic diagram of 1-digit BCD adder.	**03**
	(b)	State and prove De-Morgan's theorems using truth-tables.	**04**
	(c)	Design 3-bit even parity generator circuit.	**07**
		OR	
	(c)	Design full adder circuit using decoder and multiplexer.	**07**
Q.3	**(a)**	Design half subtractor logic circuit.	**03**
	(b)	Implement D flip flop using JK flip flop.	**04**
	(c)	Design 2 - Bit Magnitude Comparator.	**07**
		OR	
Q.3	**(a)**	Differentiate synchronous counter and asynchronous counter.	**03**
	(b)	Draw & explain in brief the logic diagram of 4-bit bidirectional shift register.	**04**
	(c)	Design a Combinational circuit that convert Binary to BCD code converter.	**07**
Q.4	**(a)**	Explain S-R clocked flip flop.	**03**
	(b)	Explain the specification of D/A converter.	**04**
	(c)	Design mod-6 asynchronous counter using T flip flop.	**07**
		OR	
Q.4	**(a)**	List out and explain any one application of the register.	**03**
	(b)	Design 4 X 16 decoder using two 3 X 8 decoders.	**04**
	(c)	Design a 3-bit synchronous up counter using JK flip-flops.	**07**
Q.5	**(a)**	Compare SRAM with DRAM.	**03**
	(b)	Draw & explain the block diagram of ALU.	**04**
	(c)	Write a short note on FPGA.	**07**
		OR	
Q.5	**(a)**	Explain classification of Memories.	**03**
	(b)	Explain R-2R ladder type D/A converter.	**04**
	(c)	Write a short note on ROM & its types.	**07**

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Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER–III (NEW) EXAMINATION – WINTER 2024

Subject Code: 3130704 **Date: 10-12-2024**

Subject Name: Digital Fundamentals

Time: 10:30 AM TO 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1*	**(a)**	(a) Perform the following mathematical operations using 2's complement method. (i) $(9)_{10} + (-5)_{10}$ (ii) $(3)_{10} - (8)_{10}$	**03**
	(b)	State and prove De-Morgan's theorems using truth-tables.	**04**
	(c)	Explain the characteristics of Digital ICs.	**07**
Q.2	**(a)**	Design a Full Adder circuit using basic logic gates.	**03**
	(b)	Design a modulo-6 ripple counter using T-Flip-flops.	**04**
	(c)	Design a 4-bit Binary to Gray Code Converter using K-map.	**07**
		OR	
	(c)	Draw a two input TTL NAND gate and explain its operation.	**07**
Q.3	**(a)**	Explain Race Around Condition in JK flip flop.	**03**
	(b)	Design a 1 - bit Magnitude Comparator.	**04**
	(c)	Explain Hamming codes for error correction with a suitable example.	**07**
		OR	
Q.3	**(a)**	Find expression for the following and implement using logic gates. $F(A,B,C,D) = \pi M(0,2,3,6,7,8,9,12,13)$	**03**
	(b)	Implement D flip flop using JK flip flop.	**04**
	(c)	Design a 4-bit twisted Ring Counter using JK flip flops.	**07**
Q.4	**(a)**	Differentiate Synchronous Counters and Asynchronous Counters.	**03**
	(b)	Implement the following using 8:1 MUX. $F = f(A,B,C,D) = \Sigma m(2,4,5,7,10,14)$	**04**
	(c)	Design a synchronous BCD counter using J-K flip-flops.	**07**
		OR	
Q.4	**(a)**	Implement full subtractor using 3:8 decoder and write a truth table.	**03**
	(b)	Explain the specifications of Digital to Analog Converters.	**04**
	(c)	Explain Successive Approximation type A/D converter.	**07**
Q.5	**(a)**	Differentiate Static RAM and Dynamic RAM.	**03**
	(b)	Write a short note on FPGA.	**04**
	(c)	Explain the operation of Dual-slope A/D converter.	**07**
		OR	
Q.5	**(a)**	Explain basic structure of a CCD (Charge Coupled Device).	**03**
	(b)	Write a short note on Programmable Array Logic.	**04**
	(c)	Explain various types of Read Only Memory.	**07**

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Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER– III(NEW) EXAMINATION – WINTER 2022

Subject Code:3130704 Date:27-02-2023

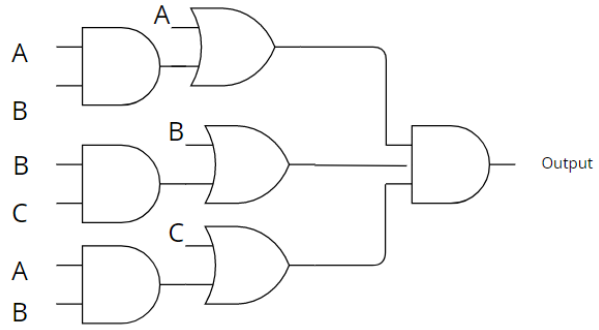
Subject Name:Digital Fundamentals

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Implement NOR, AND, & OR gates using NAND gates only	**03**
	(b)	Wrtite the boolean expression for the logic diagram given below and simplify it as much as possible and draw the logica digarm that implements the simplified expression	**04**



	(c)	Do as directed: 1. Convert $(75.75)_{10}$ = (____) $_8$ = (____)16 2. Convert $(101.10)_{16}$ = (__)$_8$ 3. Add $(17)_{10}$ and $(-25)_{10}$ using 8-bit 2's complement	**07**
Q.2	**(a)**	Explain SR flip-flop using characteristic table & characteristic equation	**03**
	(b)	Explain 4-bit parallel binary adder with neat and clean diagram	**04**
	(c)	Obtain the set of prime implicants for Function F= $\sum$ m (1,2,3,5,6,7,8,9,12,13,15)	**07**
		OR	
	(c)	A combinational logic circuit is defined by the functions: F1= Σ (0,1,2,4) and F2= Σ (0, 5, 6,7). Implement the circuit with a PLA having three inputs, four product terms and two outputs.	**07**
Q.3	**(a)**	Differentiate synchronous counter and asynchronous counter	**03**
	(b)	Explain BCD adder using two 4-bit adder IC and a correction -detector circuit	**04**
	(c)	Do the conversion of JK flip flop to T flip flop and D flip flop to JK	**07**
		OR	
Q.3	**(a)**	Design 4 X 16 decoder using two 3 X 8 decoders	**03**
	(b)	List and explain in detail Binary codes with example	**04**
	(c)	Design mod-6 asynchronous counter using T flip flop	**07**
Q.4	**(a)**	Reduce the expression Σ (2, 3, 6,7,8,10,11,14) using K-map	**03**

	(b)	Do as directed: 1. Add 25+17 in BCD 2. Add 37 +28 in XS-3	**04**
	(c)	With a neat block diagram explain the function of encoder. Explain priority encoder?	**07**
		OR	
Q.4	**(a)**	Explain R-2R ladder type D/A converter	**03**
	(b)	Implement the following Boolean functions with a 3 x 1 multiplexer F (w, x, y, z) = Σ (2, 3, 5, 6, 11, 14, 15)	**04**
	(c)	Design Combinational circuit for Binary to Xs-3 conversion	**07**
Q.5	**(a)**	Compare TTL, ECL, & CMOS logic families.	**03**
	(b)	Draw truth table of 2-bit digital comparator	**04**
	(c)	List out various commonly used D/A converters. Draw & explain any one D/A converter.	**07**
		OR	
Q.5	**(a)**	A combinational logic circuit is defined by the functions: F1= Σ (0,1,2,5,7) and F2= Σ (1, 2,4, 6). Implement the circuit with a PROM	**03**
	(b)	Explain types of shift-register and their application	**04**
	(c)	List out various commonly used A/D converters. Draw & explain any one A/D converter	**07**