Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER– III EXAMINATION – SUMMER 2026

Subject Code:3131102 Date:19-06-2026

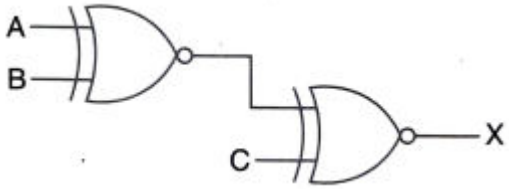
Subject Name:Digital System Design

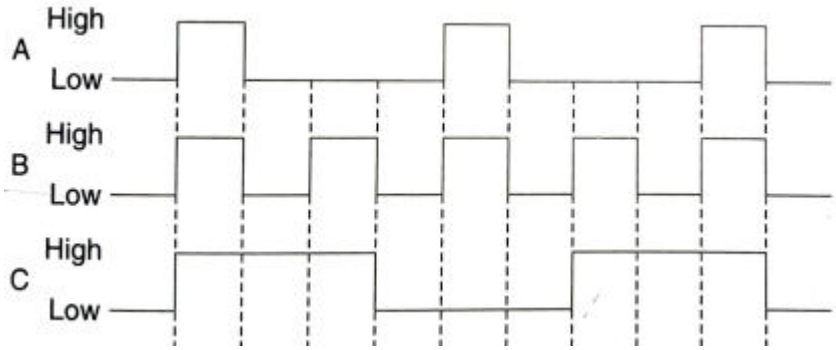
Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	What do you mean by positional weighted system. Name some positional weighted system.	**03**
	(b)	Given that $292_{10}=1204_b$ Than find the value of b.	**04**
	(c)	What are the characteristic of 2's complement numbers. What are the three methods of obtaining 2's complement of given number. Explain with suitable example.	**07**
Q.2	**(a)**	Write a short note on Gray Codes.	**03**
	(b)	If the waveforms A, B, C are applied to the gate circuit shown below, determine the output waveform.	**04**





	(c)	Write a short note on magnitude comparator.	**07**
		OR	
	(c)	Write a short note on binary full adder and implement the circuit using universal logic.	**07**
Q.3	**(a)**	How do you convert AOI logic to universal logic.	**03**
	(b)	Reduce using mapping the expression $f = \Sigma$ m (0, 1, 2, 3, 5, 8, 9,10, 12, 13)	**04**
	(c)	Explain working principal of Master Slave flip flop using suitable diagram.	**07**

OR

Q.3	**(a)**	Why do we need to reduce Boolean expression before realization. What is the systematic procedure to reduce the Boolean expression?	**03**
	(b)	Write a Short note on SR flip flop	**04**
	(c)	Explain Quine-McCluskey method for the minimization of Boolean expression.	**07**
Q.4	**(a)**	Write a short note on programmable array logic.	**03**
	(b)	Give comparison of programmable logic device such as PROM, PAL, PLA.	**04**
	(c)	Write a short note on TTL logic families.	**07**

OR

Q.4	**(a)**	Distinguished between combinational and sequential logic circuit.	**03**
	(b)	What are moore and mealy machines? Compare them.	**04**
	(c)	Write a short note on universal shift register.	**07**
Q.5	**(a)**	Write a short note on weighted resistor type D to A converter.	**03**
	(b)	Explain R-2R ladder type D to A converter.	**04**
	(c)	Explain following parameter for D to A conversion. Resolution, Accuracy, settling time, offset voltage.	**07**

OR

Q.5	**(a)**	What do you mean by test bench in VHDL design.	**03**
	(b)	List and explain the data types used in HDL	**04**
	(c)	Compare data flow ,behavioral and structural modeling.	**07**

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Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III EXAMINATION – SUMMER 2025

Subject Code:3131102 Date:31-05-2025

Subject Name:Digital System Design

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Convert the decimal Number 250.5 to base 4 and base 8.	**03**
	(b)	State and prove DeMorgan's Theorem.	**04**
	(c)	Minimize the following function in SOP and POS minimal form using K-Maps: F(A, B, C, D) =∑m(1, 2, 6, 7, 8, 13, 14, 15) + d(3, 5, 12)	**07**
Q.2	**(a)**	Convert F(A,B,C) = BC+A into standard minterm form.	**03**
	(b)	Implement Ex -NOR and Ex-OR using NAND and NOR only.	**04**
	(c)	Implement the full adder & full subtractor using Multiplexer.	**07**
		OR	
	(c)	Design and implement binary to Excess-3 code converter.	**07**
Q.3	**(a)**	Obtain the truth table of the function: F = xy+yz+zx.	**03**
	(b)	Obtain JK flip-flop from SR flip-flop.	**04**
	(c)	Draw the circuit diagrams and truth table of SR, D, T and JK flip flops.	**07**
		OR	
Q.3	**(a)**	What is "Lock out" condition in counter? How to avoid it?	**03**
	(b)	Implement 4x16 decoder using two 3x8 decoder.	**04**
	(c)	Explain Master Slave JK flip-flop with truth table and circuit diagram.	**07**
Q.4	**(a)**	Compare sequential and combinational circuits.	**03**
	(b)	Define the following characteristics of IC: (i) Propagation Delay (ii) Figure of Merit (iii) Fan out (vi) Noise Margin	**04**
	(c)	Compare ROM, PLA and PAL.	**07**
		OR	
Q.4	**(a)**	Compare Latch and a Flip flop.	**03**
	(b)	Give classification of logic families and compare CMOS and TTL.	**04**
	(c)	Explain Moore machine.	**07**
Q.5	**(a)**	List the steps in VLSI Design flow.	**03**
	(b)	Design Modulo-8 counter using T flip flop.	**04**
	(c)	With neat sketch design 4-bit bidirectional shift register.	**07**
		OR	
Q.5	**(a)**	Define State Table and State Diagram.	**03**
	(b)	Design mod-6 asynchronous counter using T flip-flop.	**04**
	(c)	Design 4-bit ripple counter using negative edge triggered JK flip flop.	**07**

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GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III (NEW) EXAMINATION – SUMMER 2024

Subject Code:3131102 **Date:29-06-2024**

Subject Name: Digital System Design

Time:10:30 AM TO 01:00 PM **Total Marks:70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Convert the decimal number 250.5 to base 3, base 7 and base 8.	**03**
	(b)	Show that NAND Gate is a Universal Gate.	**04**
	(c)	simplify the following Boolean function, F(w,x,y,z)=∑m(2,6,8,9,10,11,14,15) using Quine-McClukey tabular Method.	**07**
Q.2	**(a)**	Show that (A ⊕B ⊕C)' = (A ⊙B ⊙C).	**03**
	(b)	Obtain the truth table of the function: F= xy + xy′ + y′z.	**04**
	(c)	Minimize the logic function F (A,B,C,D)= Π_M(1, 2, 3, 8, 9, 10, 11,14) using K map & Draw the logic circuit for the simplified function using NOR gates only.	**07**
		OR	
	(c)	What is multiplexer? With logic circuit and function table explain the working of 4 to 1 line multiplexer.	**07**
Q.3	**(a)**	What is race around condition in JK flip flop?	**03**
	(b)	List out problems of asynchronous circuit. Also exemplify any two problems with suitable examples.	**04**
	(c)	With necessary sketch explain Bidirectional Shift Register with parallel load.	**07**
		OR	
Q.3	**(a)**	Implement 8x1 MUX using 4x1 MUX.	**03**
	(b)	Implement 4x16 decoder using two 3x8 decoder.	**04**
	(c)	Explain working of master-slave JK flip-flop with necessary logic diagram, state equation and state diagram.	**07**
Q.4	**(a)**	Define the terms 1. Fan out 2.Noise Margin 3. Fan in	**03**
	(b)	Design Modulo-8 counter using T flip flop.	**04**
	(c)	Explain Moore machine.	**07**
		OR	
Q.4	**(a)**	How many flip-flops are required to build a digital counter to count from 0 to 63? Justify.	**03**
	(b)	What are the classifications of Logic families? Also list the characteristics of digital IC.	**04**
	(c)	Compare ROM, PLA and PAL.	**07**
Q.5	**(a)**	List the steps in VLSI Design flow.	**03**
	(b)	Describe General State Machine Architecture with suitable diagrams.	**04**
	(c)	Design a synchronous BCD counter with JK flip-flops.	**07**
		OR	
Q.5	**(a)**	Implement T flip flop using D flip flop.	**03**
	(b)	Explain 4 bit serial in serial out shift register.	**04**
	(c)	Design 4-bit ripple counter using negative edge triggered JK flip flop.	**07**

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Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III(NEW) EXAMINATION – SUMMER 2023

Subject Code:3131102 Date:28-07-2023

Subject Name:Digital System Design

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Convert the following numbers form given base to the base indicates. (1) $(AEF2.B6)_{16} = (\_\_\_\_\_)_2$ (2) $(674.12)_8 = (\_\_\_\_\_)_{10}$ (3) $(110110.1011)_2 = (\_\_\_\_\_)_{16}$	**03**
	(b)	Sate and prove DeMorgan's Theorem.	**04**
	(c)	simplify the following Boolean function, $f(w,x,y,z)=\sum m(2,6,8,9,10,11,14,15)$ using Quine-McClukey tabular Method.	**07**
Q.2	**(a)**	Obtain canonical Sum of Product form of following function: F=AB+ACD.	**03**
	(b)	Show that NAND & NOR are universal gates.	**04**
	(c)	Implement the following Boolean functions with a multiplexer and Decoder. $F(w, x, y, z) = \Sigma (2, 3, 5, 6, 11, 14, 15)$	**07**
		OR	
	(c)	Design and implement binary to gray code converter.	**07**
Q.3	**(a)**	Implement 8x1 MUX using 4x1 MUX.	**03**
	(b)	Give the comparison between synchronous and asynchronous counters.	**04**
	(c)	Explain JK flip flop with its characteristic table and excitation table.	**07**
		OR	
Q.3	**(a)**	What is race around condition in JK flip flop?	**03**
	(b)	Implement 4x16 decoder using two 3x8 decoder.	**04**
	(c)	Explain Master Slave JK flip-flop with truth table and circuit diagram	**07**
Q.4	**(a)**	Define following terms w.r.t Digital Logic Family: 1. Figure of merit 2.Noise Margin 3. Power Dissipation	**03**
	(b)	Describe General State Machine Architecture with suitable diagrams.	**04**
	(c)	Compare ROM, PLA and PAL.	**07**
		OR	
Q.4	**(a)**	Define following terms w.r.t State Machine 1. State Table 2. State Diagram	**03**
	(b)	Give classification of logic families. Also list the characteristics of digital IC.	**04**
	(c)	Explain Moore machine.	**07**
Q.5	**(a)**	List the steps in VLSI Design flow.	**03**
	(b)	Design Modulo-8 counter using T flip flop.	**04**

	(c)	With neat sketch design 4-bit bidirectional shift register.	**07**

OR

Q.5	**(a)**	Explain the problem associate of an asynchronous state machine with the help of one example.	**03**
	(b)	Design 3-bit synchronous up counter using T flip flop.	**04**
	(c)	Design 4-bit ripple counter using negative edge triggered JK flip flop.	**07**

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