Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER–III EXAMINATION – WINTER 2025

Subject Code:3131102 Date:15-12-2025

Subject Name: Digital System Design

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Perform following subtraction using 2's complement method. $(11010)_2 - (10000)_2$	**03**
	(b)	State & prove De Morgan's theorems with the help of truth tables.	**04**
	(c)	Simplify the following Boolean expression by means of the Tabulation method. $F(A,B,C,D) = \sum m(0,1,2,4,6,8,9,11,13,15)$	**07**
Q.2	**(a)**	Converts the following nos. (i) $(52)_{10} = (\ )_2$ (ii) $(436)_8 = (\ )_{16}$ (iii) $(5C7)_{16} = ()_{10}$	**03**
	(b)	Show that $(A \oplus B \oplus C)' = (A \odot B \odot C)$	**04**
	(c)	Express Boolean function in Standard Form also Find the Minterms & Maxterms. (i) $F(A,B,C) = AB + A'C$ (ii) $F(A,B,C,D) = A + B$	**07**
		OR	
	(c)	Design a 4 bit binary to Excess-3 converter.	**07**
Q.3	**(a)**	What is race around condition in JK flip-flop.	**03**
	(b)	Design 3-bit odd parity Generator.	**04**
	(c)	Explain SR Flip-Flop circuit using its symbol, block diagram, truth table and characteristics equation.	**07**
		OR	
Q.3	**(a)**	Draw logic diagram, graphical symbol and Characteristic table for clocked D flip-flop.	**03**
	(b)	Compare ROM, PLA and PAL.	**04**
	(c)	Explain Master Slave JK flip-flop with truth table and circuit diagram.	**07**
Q.4	**(a)**	Discuss general state machine architecture.	**03**
	(b)	Implement the following expression using 8:1 mux $F(A,B,C,D)=\sum m(0,1,3,5,7,10,11,13,14,15)$.	**04**
	(c)	Draw and explain Ring counter.	**07**
		OR	
Q.4	**(a)**	Explain edge triggering and level triggering.	**03**
	(b)	Explain full adder and design a full adder circuit using 3 to 8 decoder and two OR gates.	**04**
	(c)	Design Modulo-8 counter using T flip-flop.	**07**

Q.5	**(a)**	Give comparison of TTL and CMOS family.	**03**
	(b)	Explain different modeling styles in Verilog.	**04**
	(c)	Describe the operation of Bi-directional Shift Register with parallel load With necessary logic diagram.	**07**

OR

Q.5	**(a)**	Define: i) Power dissipation ii) Noise Margin iii) Figure of merit	**03**
	(b)	Explain Moore machine.	**04**
	(c)	Write a short note on FPGA.	**07**

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Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER–III (NEW) EXAMINATION – WINTER 2024

Subject Code: 3131102 Date: 29-11-2024

Subject Name: Digital System Design

Time: 10:30 AM TO 01:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed**.

			Marks
Q.1	(a)	Convert the decimal number 345.75 to base 4, base 5, and base 9.	**03**
	(b)	Prove that NOR Gate is a Universal Gate.	**04**
	(c)	Simplify the following Boolean function, F(a,b,c,d) = ∑m(1,3,5,7,12,13,14) using the Quine-McCluskey Tabular Method.	**07**
Q.2	(a)	State De Morgan's Laws and provide a proof for them.	**03**
	(b)	Obtain the truth table of the function: F = (x + y)(x′ + z).	**04**
	(c)	Minimize the logic function F(A, B, C, D) = ΠM(0, 1, 2, 5, 8, 9, 10, 13) using K-map and draw the logic circuit for the simplified function using NOR gates only.	**07**
		OR	
	(c)	What is a multiplexer? Explain the working of a 4-to-1 multiplexer with the help of a logic circuit diagram and a truth table.	**07**
Q.3	(a)	How does the race-around condition occur in JK flip-flops, and what techniques are used to avoid it?	**03**
	(b)	What are the characteristics of JK flip-flops that differentiate them from SR and D flip-flops?	**04**
	(c)	Design a half adder and derive the full adder using half adders.	**07**
		OR	
Q.3	(a)	Distinguish between combinational and sequential logic circuits.	**03**
	(b)	How can you implement a 4x16 decoder using two 2x4 decoders?	**04**
	(c)	Explain working of master-slave JK flip-flop with necessary logic diagram, state equation and state diagram.	**07**
Q.4	(a)	Explain the problem associate of an asynchronous state machine with the help of one example	**03**
	(b)	Draw logic diagram, graphical symbol and Characteristic table for clocked D flip-flop	**04**
	(c)	Draw and explain Ring counter	**07**
		OR	
Q.4	(a)	How many flip-flops are needed to design a counter that counts from 0 to 31? Explain your reasoning.	**03**
	(b)	What are the different classifications of logic families? Compare their characteristics.	**04**
	(c)	A combinational logic circuit is defined by the functions: F1= Σ (3, 5, 6, 7) and F2= Σ (0, 2, 4, 7). Implement the circuit with a PLA having three inputs, four product terms and two outputs.	**07**

Q.5	(a)	List the steps in VLSI Design flow.	**03**
	(b)	Describe a Moore machine.	**04**
	(c)	Design a synchronous BCD counter with JK flip-flops.	**07**

OR

Q.5	(a)	Define the following: 1. Fan-in 2. Noise Margin 3. Propagation Delay	**03**
	(b)	Describe the operation of a 4-bit parallel-in parallel-out shift register.	**04**
	(c)	Design a 3-bit synchronous counter using positive edge-triggered D flip-flops.	**07**

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Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III (NEW) EXAMINATION – WINTER 2023

Subject Code:3131102 Date:18-01-2024

Subject Name:Digital System Design

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Briefly explain the steps for VLSI design flow.	**03**
	(b)	Implement Full Adder using 3×8 decoder.	**04**
	(c)	Design BCD to Excess-3 code converter.	**07**
Q.2	**(a)**	Explain NAND SR Latch.	**03**
	(b)	Reduce the following expression using K-map. Σ (2, 3, 6,7,8,10,11,14)	**04**
	(c)	Explain dual slope type A/D converter in detail.	**07**
		OR	
	(c)	Design 2-bit magnitude comparator.	**07**
Q.3	**(a)**	Compare synchronous and asynchronous counter.	**03**
	(b)	Obtain JK flip-flop from SR flip-flop.	**04**
	(c)	Design a 3-bit synchronous counter using JK flip-flop.	**07**
		OR	
Q.3	**(a)**	Compare TTL, ECL, & CMOS logic families.	**03**
	(b)	Discuss general state machine architecture.	**04**
	(c)	Design mod-6 asynchronous counter using T flip-flop.	**07**
Q.4	**(a)**	Compare asynchronous and synchronous state machines.	**03**
	(b)	Explain working of D flip-flop with characteristic table and logic diagram.	**04**
	(c)	Implement the following using MUX: a) $F(A,B,C) = \sum(1,3,6)$ b) $F(A,B,C) = \pi(2,3,5)$	**07**
		OR	
Q.4	**(a)**	Define Noise margin, Propagation delay, fan-in and fan-out	**03**
	(b)	State and prove De Morgan's theorem.	**04**
	(c)	Describe working principle of Programmable Logic Array with block diagrams.	**07**
Q.5	**(a)**	Explain half subtractor with logic circuit.	**03**
	(b)	Explain minterms and maxterms.	**04**
	(c)	Describe the operation of 4-bit bidirectional shift register with logic diagram.	**07**
		OR	
Q.5	**(a)**	Compare sequential and combinational circuits.	**03**
	(b)	Discuss working fundamentals behind FINFET.	**04**
	(c)	Explain Universal Gates.	**07**

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Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER– III(NEW) EXAMINATION – WINTER 2022

Subject Code:3131102 Date:24-02-2023

Subject Name:Digital System Design

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	State and prove De-Morgan's Theorem.	**03**
	(b)	Differentiate between combinational and sequential circuits.	**04**
	(c)	Simplify the following Boolean expression by means of the Tabulation method. $F(A,B,C,D) = \sum m(1,2,5,6,7,8,9,11,12,13,15)$	**07**
Q.2	**(a)**	Convert as below I. $(110101010)_2 = (\ )_8 = (\ )_{16}$ II. $(673.10)_8 = (\ )_2$ III. $(ABF)_{16} = (\ )_{10}$	**03**
	(b)	Show that NAND & NOR are universal gates	**04**
	(c)	Minimize the following function in SOP minimal form using K-Maps: $F(A, B, C, D) = \sum m(1, 2, 6, 7, 8, 13, 14, 15) + d(3, 5, 12)$	**07**
		OR	
	(c)	Design a 4 bit binary to gray code converter and implement using EX-OR gates only.	**07**
Q.3	**(a)**	Give comparison of TTL and CMOS family.	**03**
	(b)	Explain half adder & half subtractor circuit.	**04**
	(c)	Explain about JK & RS Flip Flop circuit using its symbol, block diagram, truth table and characteristics equation.	**07**
		OR	
Q.3	**(a)**	Derive excitation tables for R-S, J-K and T flip-flops.	**03**
	(b)	Compare ROM, PLA and PAL.	**04**
	(c)	Design a counter to generate the repetitive sequence 0,1,2,4,3,6.	**07**
Q.4	**(a)**	Discuss general state machine architecture	**03**
	(b)	Implement the 8× 1 MUX using two 4 ×1 MUX.	**04**
	(c)	Describe working principle of Programmable Logic Array with block diagrams.	**07**
		OR	
Q.4	**(a)**	Define: Register, Ripple counter, Synchronous counter.	**03**
	(b)	Implement Full Adder using 3×8 decoder.	**04**
	(c)	Explain the types Finite machines.	**07**

Q.5	**(a)**	Compare asynchronous and synchronous state machines.	**03**
	(b)	Implement T flip flop using D flip flop.	**04**
	(c)	Describe the operation of 4-bit bidirectional shift register with logic diagram.	**07**

OR

Q.5	**(a)**	Define: i) Fan-in ii) Fan-out iii) Propagation delay	**03**
	(b)	Explain working of Toggle flip-flop with characteristic table and logic diagram.	**04**
	(c)	Explain dual slope type A/D converter in detail.	**07**

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