Seat No./Enrollment No.: _____

GUJARAT TECHNOLOGICAL UNIVERSITY
BACHELOR OF ENGINEERING – SEMESTER 5 – EXAMINATION – SUMMER 2026

Subject Code: 3151105 **Date: 30/05/2026**

Subject Name: VLSI Design

Time: 02:30 PM TO 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

Q.1	**(a)**	Draw VLSI Design Flow y chart and flow chart.	**03**
	(b)	Define Regularity, Modularity and Locality	**04**
	(c)	Derive threshold voltage equation of MOSFET	**07**
Q.2	**(a)**	Compare Full custom, Semi-custom and Fully Programmable VLSI design style.	**03**
	(b)	Compare Constant field and constant voltage Scaling techniques of MOSFET.	**04**
	(c)	Explain Fabrication of n-MOSFET with neat sketch.	**07**
		OR	
Q.2	**(c)**	Derive drain current using gradual channel approximate	**07**
Q.3	**(a)**	Draw VTC of practical Inverter and define all critical voltages	**03**
	(b)	Draw resistive load inverter and Derive V_{IH} critical voltage equation of it.	**04**
	(c)	Consider a resistive-load inverter circuit with V_{DD}=5V, kn'= 20 uA/V^2, V_{T0}= 0.8 V, R_L = 200 kΩ, and W/L = 2. Find noise margin high MN_H.	**07**
		OR	
Q.3	**(a)**	What is need of Design of Testability and Define Controllability and observability	**03**
	(b)	Draw CMOS inverter and Derive V_{IL} critical voltage equation of it.	**04**
	(c)	Consider a CMOS inverter with the following parameters: VTon = 0.6 V, VTop = -0.7 V, Kn = 200 uA/V^2, Kp = 80 uA/V^2 and VDD = 3.3 V. Find noise margin low NM_L.	**07**
Q.4	**(a)**	Draw three stage ring oscillator circuit and derive it generated signal frequency equation	**03**
	(b)	Realize the following Boolean function using Transmission Gate: F=AB+A'C'+AB'C	**04**
	(c)	Draw i/p and o/p waveform during high to low transition of o/p for CMOS inverter and derive expression for ζ_{PHL}. Using differential equation method	**07**
		OR	
Q.4	**(a)**	Draw the circuit diagram of domino CMOS logic gate	**03**
	(b)	Draw CMOS implementation of D latch with two inverters and two CMOS TG gates.	**04**
	(c)	Derive switching power dissipation equation of CMOS inverter with idea step input.	**07**

Q.5	**(a)**	Compare FinFET and Planar MOSFET	**03**
	(b)	What is the need of voltage bootstrapping? Draw voltage bootstrapping circuit.	**04**
	(c)	What is clock skew. Draw and Explain on chip clock generation and distribution circuits.	**07**

OR

Q.5	**(a)**	Implement clocked JK latch using CMOS inverter.	**03**
	(b)	Explain latch up problem in CMOS inverter. Mention causes and remedy for avoiding latch up.	**04**
	(c)	Write a short note on Built In Self Test(BIST).	**07**

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Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–V EXAMINATION – SUMMER 2025

Subject Code:3151105 Date:20-05-2025

Subject Name:VLSI Design

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Present device isolation techniques in fabrication process.	**03**
	(b)	Explain the MOS system under external bias.	**04**
	(c)	Describe the working of edge-triggered flip-flops with necessary diagrams.	**07**
Q.2	**(a)**	Explain the basic principles of pass transistor circuits.	**03**
	(b)	Design 2-input OR, AND and XOR gate using CMOS.	**04**
	(c)	Present the analysis of the resistive load inverter. Derive critical voltages and noise margins.	**07**
		OR	
	(c)	Analyze transmission gates (TGs) in detail. Also, describe the procedure for circuit design with TGs.	**07**
Q.3	**(a)**	Enlist MOSFET scaling and small-geometry effects.	**03**
	(b)	Discuss synchronous dynamic circuit techniques.	**04**
	(c)	Present timing analysis of CMOS inverter.	**07**
		OR	
Q.3	**(a)**	What is the built-in self-test (BIST)? Explain this technique in brief.	**03**
	(b)	Describe the behavior of bistable elements.	**04**
	(c)	Explain voltage bootstrapping.	**07**
Q.4	**(a)**	Write the equations describing the current-voltage characteristics of MOSFET.	**03**
	(b)	Describe fabrication of nMOS Transistor.	**04**
	(c)	Analyze the factors behind latch-up problems. Also, explain the techniques for its prevention.	**07**
		OR	
Q.4	**(a)**	What is the substrate bias effect? Explain its analysis.	**03**
	(b)	Discuss switching power dissipation of CMOS inverters.	**04**
	(c)	Present the analysis of on-chip clock generation and distribution techniques.	**07**
Q.5	**(a)**	Define and explain DIBL.	**03**
	(b)	Present delay-time definitions.	**04**
	(c)	Discuss fault types and models.	**07**
		OR	
Q.5	**(a)**	Explain controllability and observability.	**03**
	(b)	Describe the operating principle of the SR latch circuit with the necessary diagrams.	**04**
	(c)	What are the needs of FinFET devices? Explain FinFET devices in detail. Also, compare them with planar MOSFET.	**07**

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Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–V (NEW) EXAMINATION – SUMMER 2024

Subject Code:3151105 Date:23-05-2024

Subject Name:VLSI Design

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Compare semicustom and Full custom VLSI design style.	**03**
	(b)	Discuss following approaches used to reduce complexity of IC design i) Hierarchy ii) Regularity iii) Modularity iv) Locality	**04**
	(c)	Draw and explain various fabrication steps for CMOS inverter with proper notations at each fabrication steps.	**07**
Q.2	**(a)**	Explain MOSFET capacitance in brief.	**03**
	(b)	Derive the drain current equation for MOSFET using Gradual Channel Approximation (GCA)	**04**
	(c)	Find the depletion layer width, depletion region charge and threshold voltage with no substrate bias with the following physical parameters. Physical parameters VSB=0, for silicon gate n channel MOS transistor, with the following parameters: Substrate doping density NA=1.5 x 10^{16} cm^{-3}, Gate donor doping N_D = 10^{18} cm^{-3}, Gate oxide thickness tox = 400A°, Nss = 10 x 10^{10} cm^{-3}. Consider Boltzmann Constant = 1.38 x10^{-23} (J/K), Electron charge = 1.6 x 10^{-19} C, Intrinsic Silicon carrier concentration ni= 1.45 x 10^{10} cm^{-3}, $\varepsilon_S i$ = 1.035 x 10^{-12} F/cm ε_0 = 8.85x10^{-14} F/cm, εox = 0.345 x 10^{-12} F/cm.	**07**
		OR	
	(c)	For an enhancement type NMOS transistor has its source terminal connected to ground and 3 V connected to ground and 3 V connected to the gate. NMOS has V_T= 2 V , λ= 0.04 1/V , μ_n *C_{ox}=20A/V^2, W= 200μm and L =10μm , V_G= 3V , V_D=0.5 V and 1 V. Calculate Drain Current I_D. **Physical constants** : Thermal voltage =KT/q = 0.026 volt. Energy Gap of silicon (Si) =E_g = 1.12 Ev. Intrinsic Carrier Concentration of silicon=n_i=1.45x$10^{10}$$cm^{-3}$. Dielectric constant of vaccume =ε_o=8.85 x 10-^{14}F/cm. Dielectric constant of silicon =ε_{si}= 11.7 xε_oF/cm. Dielectric constant of silicon dioxide =ε_{ox}= 3.97 xε_oF/cm	**07**
Q.3	**(a)**	What is meant by static and dynamic power dissipation?	**03**

(b) Define propagation delay and derive the expression for τpHL for CMOS inverter. Assume ideal step as an input to CMOS inveter. **04**

(c) Consider a resistive load inverter circuit with V_{DD}=5 V, Kn' =10μA/V^2 V_{TO}=0.8V,RL=400kΩ and W/L=2.Calculate the critical Voltages (V_{OH},V_{OL},V_{IL} and V_{IH}) on the VTC and find the noise margins of the circuit. **07**

OR

Q.3 **(a)** Draw CMOS inveter. Explain its voltage transfer characteristic. Also explain the NML and NMH noise margins with respect to this transfer characteristic **03**

4.4.13

(b) Draw the inverter circuit with depletion type nMOS load. Mention the operating regions of driver and load transistors for different input voltages. Derive critical voltage points V_{OH}, V_{OL} , V_{IH} and V_{IL} for depletion- load nMOS inverter **04**

(c) Consider a CMOS inverter with the following parameters: **07**
VDD=3.3 V, $VT0,n$= 0.6 V, $VT0,p$= −0.7 V ,kn= 200 $\mu A/V^2$ and kp= 160 $\mu A/V^2$
Calculate the noise margins of the circuit. Consider k_R=2.5 V and $V_{T0,}\neq|V_{T0,p}|$ as it is not a symmetric CMOS inverter.

Q.4 **(a)** What are the limitations of Dynamic circuits? Discuss the effect of charge sharing and charge leakage in dynamic pass transistor logic. **03**

(b) Two nMOS transistors (M1 and M2) connected in series is shown in Figure 1. The power supply is VDD =3.3 V and the nMOS threshold V_{TN} = 0.55 V. Find the output voltage at node b. Consider i) Va = 2.7 V and ii) Va = 3V. **04**

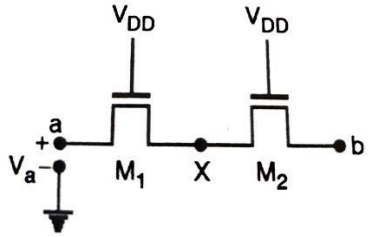


Figure 1

(c) Explain the Euler path approach to find the optimized stick-diagram for any CMOS logic circuit. Draw the optimized stick-diagram for the following Boolean function (CMOS Logic), F= (A(D+E)+ BC)'. Explain the importance of Euler path approach. **07**

OR

Q.4 **(a)** What do you mean by stick diagram? Implement the following Boolean function using stick diagram. **03**
Y = (A*(D+E)+B*C)'

(b) Explain the need of Voltage bootstrapping? Derive the mathematical expression for dynamic Voltage bootstrapping circuit. **04**

(c) For the Exclusive OR function , draw with following realization **07**

1. Static CMOS realization
2. Pseudo nMOS gate
3. CMOS Transmission Gate(TG)

Q.5 **(a)** Compare FinFET and Planner MOSFET **03**

(b) Draw transistor level circuit diagram of NAND based SR latch using CMOS. **04**

	(c)	What is clock-skew? Explain on-chip clock generation and distribution.	**07**
		OR	
Q.5	**(a)**	Draw and discuss three stage ring oscillator	**03**
	(b)	Implement and Describe CMOS clocked SR flip-flop	**04**
	(c)	What is need of Design of Testability (DFT) in VLSI IC design and explain Built in Self Test (BIST) techniques of DFT	**07**

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Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE – SEMESTER- V EXAMINATION-SUMMER 2023

Subject Code: 3151105 Date: 28/06/2023

Subject Name: VLSI Design

Time: 02:30 PM TO 05:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

Q.1	**(a)**	What is the role of photo resist material in IC fabrication process?	**03**
	(b)	Describe concepts of Regularity and Modularity.	**04**
	(c)	What is the impact of different VSLI Design styles upon the design cycle time and achievable circuit performance?	**07**
Q.2	**(a)**	Compare constant voltage scaling and constant field scaling.	**03**
	(b)	Note down physical parameters affecting the threshold voltage of MOS structure.	**04**
	(c)	Write down basic steps of Local oxidation of Silicon (LOCOS) process.	**07**
		OR	
	(c)	What is channel length modulation? How it affects drain current of MOSFET?	**07**
Q.3	**(a)**	Define: Propagation delay, Rise time and Fall time.	**03**
	(b)	What is hot carrier effect and punch through in small geometries devices?	**04**
	(c)	Explain the junction capacitances associated with MOS structure.	**07**
		OR	
Q.3	**(a)**	Discuss 3 stage CMOS ring oscillator circuit with necessary waveforms.	**03**
	(b)	Explain: Body effect and Noise margin.	**04**
	(c)	Give the comparison of resistive load, depletion load and CMOS inverter circuits.	**07**
Q.4	**(a)**	Draw transmission gate implementation of XOR gate.	**03**
	(b)	Show with the diagram, bias conditions and operating regions of CMOS transmission gate, as a function of output voltage.	**04**
	(c)	In CMOS inverter circuit, define propagation delay τ_{PLH} (low-to-high transition at output) and obtain its expression.	**07**
		OR	
Q.4	**(a)**	Draw CMOS implementation of D latch.	**03**
	(b)	Explain basic principles of Pass transistor circuits.	**04**
	(c)	Draw CMOS circuit for NAND gate and derive threshold voltage equation for it.	**07**
Q.5	**(a)**	Explain cascading problem in dynamic CMOS logic.	**03**
	(b)	Draw and explain the basic circuit architecture of Zipper CMOS circuits with clock signals.	**04**
	(c)	Differentiate the ratioed and ratio less dynamic logic circuits with examples.	**07**
		OR	
Q.5	**(a)**	Give examples of physical defects.	**03**
	(b)	Explain controllability and Observability.	**04**
	(c)	What is latch up in CMOS circuits and how it can be prevented?	**07**

Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–V(NEW) EXAMINATION – SUMMER 2022

Subject Code:3151105 Date:13/06/2022

Subject Name:VLSI Design

Time:02:30 PM TO 05:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Define concept of : Modularity, Locality and Regularity	**03**
	(b)	Explain accumulation, depletion and inversion of MOS under external bias.	**04**
	(c)	Explain process flow of fabrication of nMOS transistoron p-type silicon.	**07**
Q.2	**(a)**	Explain in short: FPGA	**03**
	(b)	What is transmission gate?	**04**
	(c)	Derive MOSFET current -voltage characteristics using gradual channel approximation.	**07**
		OR	
	(c)	Measured voltage and current data for a MOSFET are given below: Determine the type of the device and calculate the parameters k_n, V_{TO}, and γ. Assume φ_F = -0.3V. Assume MOSFET is enhancement type and neglect channel length modulation effect.	**07**

V_{GS}**(V)**	V_{DS}(V)	V_{SB}(V)	I_D (μa)
3	3	0	97
4	4	0	235
5	5	0	433
3	3	3	59
4	4	3	173
5	5	3	347

Q.3	**(a)**	Explain noise margin.	**03**
	(b)	Explain rise time and fall time of inverter using diagram.	**04**
	(c)	Consider a resistive load inverter circuit with V_{DD}= 5V, k_n' =20μA/V^2, V_{TO} = 0.8V, R_L = 200kΩ and W/L =2. Calculate critical voltages (V_{OL}, V_{OH}, V_{IL}, V_{IH}) and find the noise margins of the circuit.	**07**
		OR	
Q.3	**(a)**	Explain voltage transfer characteristics of inverter.	**03**
	(b)	Explain propagation delay time for inverter: τ_{PLH}, τ_{PHL}	**04**
	(c)	Explain CMOS inverter and find equation of V_{IL} and V_{IH}.	**07**
Q.4	**(a)**	Explain different fault types in chip.	**03**
	(b)	Explain two input CMOS NOR gate.	**04**
	(c)	Explain Elmore delay with suitable diagram.	**07**
		OR	
Q.4	**(a)**	What is latch-up? Write causes of latch- up.	**03**

	(b)	Draw CMOS implementation of XOR function.	**04**
	(c)	Explain CMOS ring oscillator circuit.	**07**
Q.5	**(a)**	Explain Controllability and Observability.	**03**
	(b)	Design CMOS SR latch circuit based on NOR gate.	**04**
	(c)	Explain Domino CMOS logic.	**07**

OR

Q.5	**(a)**	Compare FinFET and Planner MOSFET.	**03**
	(b)	Explain CMOS implementation of D - latch.	**04**
	(c)	Explain voltage bootstrapping.	**07**

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