Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER–V EXAMINATION – WINTER 2025

Subject Code:3151105 Date:25-11-2025

Subject Name:VLSI Design

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	What is chip reliability? List the four major causes of chip reliability issues.	**03**
	(b)	Explain the channel length modulation effect in n-channel MOSFET operation.	**04**
	(c)	Explain the MOS system under external bias for accumulation and depletion region.	**07**
Q.2	**(a)**	What is substrate bias effect?	**03**
	(b)	Compare and explain the full custom and semi-custom design style of VLSI.	**04**
	(c)	Draw and explain the basic steps of Local oxidation of Silicon (LOCOS) process.	**07**
		OR	
	(c)	Explain the process steps for fabrication of n-channel MOSFET.	**07**
Q.3	**(a)**	Explain RC delay models for calculation of interconnect delay.	**03**
	(b)	For depletion load n MOS inverter circuit, derive the equation of V_{IL}.	**04**
	(c)	Consider the CMOS inverter circuit with following parameters: V_{DD} = 3.3V, k_n =200 μA/V^2, k_p =80 μA/V^2, $V_{TO,n}$ = 0.6V, $V_{TO,p}$ = -0.7V. Calculate the V_{IL} and V_{OH} on the VTC of the inverter.	**07**
		OR	
Q.3	**(a)**	Draw the circuit of 2 input CMOS NAND gate and explain its working with the help of truth table.	**03**
	(b)	Why in symmetrical and ideal CMOS inverter required (W/L)p ≈ 2.5 (W/L)n ? Explain in detail.	**04**
	(c)	Consider a resistive load inverter circuit with V_{DD}= 5V, k'$_n$ =20μA/V^2, V_{TO} = 0.8V, R_L = 200 kΩ and W/L =2. Calculate V_{OL} and V_{IH} on the VTC of the inverter.	**07**
Q.4	**(a)**	Explain AOI (AND-OR-INVERT) and OAI (OR-AND-INVERT) circuit categories with example for CMOS logic.	**03**
	(b)	Derive switching power dissipation equation of CMOS inverter.	**04**
	(c)	How logic "1" transfer happens in nMOS pass transistor circuits. Explain with suitable example.	**07**
		OR	
Q.4	**(a)**	Draw the AOI based implementation of the clocked NOR based SR latch circuit.	**03**
	(b)	Implement XOR function using CMOS TG (Transmission Gates).	**04**

	(c)	Explain various on chip clock generation circuits and distribution networks.	**07**

Q.5	**(a)**	Draw the CMOS implementation of D-latch.	**03**
	(b)	What is controllability and observability for design for testability (DFT)?	**04**
	(c)	How pre-charge and evaluate logic works for dynamic CMOS circuit? Explain with example.	**07**

OR

Q.5	**(a)**	Compare FinFET and Planner MOSFET.	**03**
	(b)	Explain scan-based techniques for DFT with one example.	**04**
	(c)	Define propagation delay τ_{PHL} and obtain its expression for CMOS inverter circuit.	**07**

Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER–V (NEW) EXAMINATION – WINTER 2024

Subject Code:3151105 Date:05-12-2024

Subject Name:VLSI Design

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Draw VLSI design flow Y chart.	**03**
	(b)	Draw voltage transfer characteristics of ideal and practical inverter and define V_{IL}, V_{IH}, V_{OL}, V_{OH}, NM_L and NM_H.	**04**
	(c)	Derive threshold voltage equation and explain what is substrate bias effect?	**07**
Q.2	**(a)**	Compare full-custom, semi-custom and programmable VLSI design style.	**03**
	(b)	What is photo lithography? Differentiate positive and negative photo resist material.	**04**
	(c)	Derive MOSFET current -voltage characteristics using gradual channel approximation.	**07**
		OR	
	(c)	Explain MOS System under External Bias with neat sketch of cross sectional view and energy band diagram and derive depletion region depth equation.	**07**
Q.3	**(a)**	What is the need of Scaling? Compare constant field and constant voltage scaling.	**03**
	(b)	Draw resistive load inverter. Derive V_{OL} and V_{IL} critical voltages equation of resistive load inverter.	**04**
	(c)	Consider resistive-load inverter with R_L = 200 kΩ. The enhancement-type nMOS driver transistor has the following parameters V_{DD} = 5 V, V_{TO}= 0.8V μnCox = 20 μA/V^2 , W/L= 2. Determine V_{OL}, V_{IL} and NM_L.	**07**
		OR	
Q.3	**(a)**	Enlist advantages and disadvantages of FinFET over Planner MOSFET	**03**
	(b)	Draw CMOS inverter with leads name of pMOS and nMOS transistors. Derive V_{IL} critical Voltage equation of CMOS inverter	**04**
	(c)	Consider a CMOS inverter circuit with the following parameters: V_{DD} =3.3V, V_{TON} =0.6 V, V_{TOP}= -0.7 V, kn = 200 μA/V^2 , kp = 80 μA/V^2 , find the NM_L	**07**
Q.4	**(a)**	Implement following Boolean expression using CMOS inverter. Z= (A(D+E)+BC)'	**03**
	(b)	Realize following Boolean logic equation using Transmission Gate (TG). F = XY+ X'Z'+XY'Z	**04**

	(c)	Derive the equation for propagation delay of output signal during high to low transition of output of CMOS inverter circuit with Cload as load capacitance.	**07**

OR

Q.4	**(a)**	Draw CMOS ring oscillator and its out waveform. Write generated frequency equation.	**03**
	(b)	Construct D latch using CMOS inverters and Transmission Gates.	**04**
	(c)	Explain interconnect delay analysis using Elmore Delay model.	**07**
Q.5	**(a)**	Define controllability and observability	**03**
	(b)	Design CMOS SR latch circuit based on NOR gate.	**04**
	(c)	Explain voltage bootstrapping and derive capacitance ratio equation?	**07**

OR

Q.5	**(a)**	What is need of domino CMOS logic circuit and draw it's circuit diagram.	**03**
	(b)	What is clock skew. Draw different clock distribution networks	**04**
	(c)	Write a short note on CMOS Transmission gate.	**07**

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GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–V (NEW) EXAMINATION – WINTER 2023

Subject Code:3151105 Date:13-12-2023

Subject Name:VLSI Design

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**
5. **Note: Use following parameters for computation if required.**
   Boltzmann constant = 1.38×10^{-23} (J/K), q = 1.6×10^{-19} C, $n_i = 1.45 \times 10^{10}$ cm^{-3}, $\varepsilon_{Si} = 11.7\varepsilon_0$, $\varepsilon_0 = 8.85\times10^{-14}$ F/cm , $\varepsilon_{ox} = 3.97\varepsilon_0$ F/cm

			Marks
Q.1	**(a)**	Identify following statements are True or False. Make correction if false and justify. (i) NMOS is constructed on n type and PMOS is constructed on p type substrate. (ii) If substrate is connected with V_{DD} then threshold voltage $V_T = V_{T0}$ (iii) If V_{DS} is constant and V_{GS} increases then current I_{DS} in NMOS transistor will increase.	**03**
	(b)	For MOS structure, derive the expression for the maximum possible depth of the depletion region.	**04**
	(c)	Draw cross section of n-channel MOSFET. Obtain drain current expression as a function of V_{GS}, V_{DS}, and V_{BS} for linear and saturation region of operation of MOSFET device.	**07**
Q.2	**(a)**	Answer the following questions. (i) Which material is used for gate formation of CMOS transistor? (ii) What is feature size? (iii) Among BJT and MOS which device is smaller in size?	**03**
	(b)	Describe usage of photo resist in lithography process.	**04**
	(c)	Explain two types of scaling with its advantages and disadvantages.	**07**
		OR	
	(c)	Draw circuit of resistive load inverter. Derive expression for V_{IH}, V_{IL}, V_{OL} and V_{OH} for resistive load inverter.	**07**
Q.3	**(a)**	Consider a p-channel MOSFET with parameters $\mu_p = 300$ cm^2/V-s, $C_{ox} = 6.9 \times 10^{-8}$ F/cm^2, $(W/L) = 10$, and $V_{TP} = -0.65$V. Determine the maximum current at $V_{GS} = -3$V.	**03**
	(b)	Derive expression of threshold voltage for CMOS inverter.	**04**
	(c)	Consider reverse biased abrupt silicon p-n junction. The doping density of the n-type region is $N_D = 10^{19}$ cm^{-3} and the doping density of the p-type region is given as $N_A = 10^{16}$ cm^{-3}. The junction area is A = 20µm x 20µm. Calculate the built-in junction potential and zero bias junction capacitance per unit area for the structure.	**07**
		OR	
Q.3	**(a)**	Discuss methods to estimate interconnect parasitic.	**03**
	(b)	Explain switching power dissipation of CMOS inverter.	**04**

	(c)	Calculate the threshold voltage V_{TO} and substrate bias coefficient at $V_{SB}=0$, for silicon gate n-channel MOS transistor, with the following parameters: substrate doping density $N_A=3\times10^{16}$ cm-3, $N_D = 4\times10^{19}$ cm-3, gate oxide thickness tox = 200A°, and oxide interface fixed charge density Nox = 10^{10} cm^{-2}. Assume $\phi_{F(gate)}$ = 0.56V.	**07**
Q.4	**(a)**	Draw diagram of FinFET and discuss its advantages.	**03**
	(b)	Draw diagram of ring oscillator. For five stage ring oscillator circuit, derive expression for frequency of oscillation.	**04**
	(c)	What is need of design for testability? Explain Adhoc testable design techniques and built-in SelfTest (BIST) techniques.	**07**
		OR	
Q.4	**(a)**	List packaging technology used for VLSI chips.	**03**
	(b)	Draw the optimized stick diagram for the following function (CMOS logic) using Euler path approach, $X = \overline{ADF + B(E + C)}$	**04**
	(c)	Draw CMOS negative edge triggered master slave D flip flop and explain its working with proper circuit diagram.	**07**
Q.5	**(a)**	List examples of physical defects during chip fabrication.	**03**
	(b)	Draw 2 input NAND gate using complementary pass transistor logic.	**04**
	(c)	What is importance of CMOS Transmission gate? Draw 2×1 MUX using compound gate and compare it with 2×1 MUX based on transmission gate. Also draw 4×1 MUX based on transmission gate.	**07**
		OR	
Q.5	**(a)**	Realize XOR gate using CMOS transmission gate.	**03**
	(b)	Explain the need of Voltage bootstrapping? Derive the mathematical expression for dynamic Voltage bootstrapping circuit.	**04**
	(c)	Draw and explain 'Y' chart for the VLSI design flow.	**07**

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GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–V (NEW) EXAMINATION – WINTER 2022

Subject Code:3151105 Date:13-01-2023

Subject Name:VLSI Design

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

Q.1	**(a)**	What is reliability of the chip? List the 4 major causes for chip reliability problems.	**03**
	(b)	Explain the impact of full-custom and semi-custom VLSI design style on design cycle time and circuit performance.	**04**
	(c)	Explain the process steps for fabrication of n-type MOSFET.	**07**
Q.2	**(a)**	Draw the VTC of resistive load inverter circuit and show the 3 different operating regions of MOSFET of the circuit on it.	**03**
	(b)	What is channel length modulation effect?	**04**
	(c)	Explain the MOS system under external bias for accumulation and inversion region.	**07**
		OR	
	(c)	Derive the drain current I_D equation for n-type MOSFET using gradual channel approximation.	**07**
Q.3	**(a)**	Elaborate different clock distribution network.	**03**
	(b)	Draw and explain the operation of two input multiplexer using CMOS transmission gates.	**04**
	(c)	Derive the equation of V_{IL} and V_{IH} for CMOS inverter.	**07**
		OR	
Q.3	**(a)**	What is Latch-up in CMOS chip?	**03**
	(b)	For the function $Z = \overline{A(D+E) + BC}$. Construct dual pull up graph from pull down graph using Dual Graph Concept.	**04**
	(c)	Consider a CMOS Inverter circuit with the following parameters: V_{DD}= 3.3V, $V_{TO,n}$ = 0.6V, $V_{TO,p}$ = - 0.7V, k_n = 400 μA/V^2, k_p =160 μA/V^2 . Find the value of V_{IL}.	**07**
Q.4	**(a)**	Explain constant field scaling for MOSFET.	**03**
	(b)	Illustrate the RC delay models for calculation of interconnect delay.	**04**
	(c)	Derive the equation for propagation delay of output signal during high to low transition of output of CMOS inverter circuit with C_{load} as load capacitance.	**07**
		OR	
Q.4	**(a)**	Draw the circuit of dynamic D-latch.	**03**
	(b)	What are controllability and observability? Discuss in brief.	**04**
	(c)	Explain the working of clocked NOR based SR latch with gate level circuit and waveform. Draw the AOI based implementation of this circuit.	**07**
Q.5	**(a)**	What are the advantages of FinFET over planner MOSFET?	**03**
	(b)	What is substrate bias effect? For two input depletion load NAND gate, how many MOSFET have this effect?	**04**

	(c)	How pre-charge and evaluate logic works for dynamic CMOS circuit? Explain with example.	**07**

OR

Q.5	**(a)**	How partition and Mux technique is used to increase the testability of circuits?	**03**
	(b)	Draw and explain the basic structure of FinFET device.	**04**
	(c)	Explain NORA CMOS logic and its advantages.	**07**

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