Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III EXAMINATION – SUMMER 2025

Subject Code:3130704 Date:06-06-2025

Subject Name:Digital Fundamentals

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	State and Apply DeMorgan's theorem.: [(x+y)'+(x+y)']'=x+y	**03**
	(b)	Do As Directed: 1. Convert $(0.6875)_{10}$ to Binary. 2. Give the octal equivalent of hexadecimal numbers of DC.BA. 3. Convert $(101101.1101)_2$ to Hexadecimal. 4. Give the Truth Table of XOR gate.	**04**
	(c)	Prove that NAND and NOR gates are universal gates.	**07**
Q.2	**(a)**	Determine the value of base x if $(211)_x = (152)_8$	**03**
	(b)	Subtract $(111001)_2$ from $(101011)_2$ using 1's complement	**04**
	(c)	Simplify and implementation the following SOP function using NOR gates F(A,B,C,D)= ∑m(0,1,4,5,10,11,14,15)	**07**
		OR	
	(c)	Simplify the Boolean expression using K-map and implement using NAND gates F(A,B,C,D) = ∑m(0,2,3,8,10,11,12,14)	**07**
Q.3	**(a)**	Design the combinational circuit of 4 Bit Parallel Adder.	**03**
	(b)	Implement the following Boolean function using 8:1 multiplexer: F(A, B, C, D) = A'BD' + ACD + A'C' D +B'CD	**04**
	(c)	Design a combinational circuit with four input lines that represent a decimal digit in BCD and four output lines that generate the 9's complement of the input digit.	**07**
		OR	
Q.3	**(a)**	Design Truth table for the Half adder and write the expression for the sum and carry.	**03**
	(b)	Implement the following Boolean function using 8:1 multiplexer: F(A,B,C,D) = Σm (0,3,4,7,8,9,13,14)	**04**
	(c)	Design 5 to 32 line decoder using 3 to 8 line decoder and 2 to 4 line decoder.	**07**
Q.4	**(a)**	Explain about Ring counter.	**03**
	(b)	Describe how T flip-flop is converted into D flip-flop.	**04**
	(c)	What is the function of shift register? With the help of simple diagram explain its working.	**07**
		OR	
Q.4	**(a)**	Explain various applications of the register.	**03**
	(b)	Describe how JK flip-flop is converted into D flip-flop.	**04**
	(c)	Draw the state diagram of BCD ripple counter, develop its logic diagram and explain its operation.	**07**

Q.5	**(a)**	Write difference between PROM, PLA & PAL.	**03**
	(b)	Using 8x4 ROM, realize the expressions W(A,B,C) =∑m(0,1,3,5,7) ,X(A,B,C) =∑m(0,2,4,5) , Y(A,B,C) =∑m(1,2,4,7) , Z(A,B,C=∑m(0,3,5,6,7). Show the data at address 2 & 6.	**04**
	(c)	Implement the following function using PLA F1= ∑m(0,2,5,8,9,11),F2=∑m(1,3,8,10,13,15),F3=∑m(0,1,5,7,9,12,14).	**07**

OR

Q.5	**(a)**	Discuss : Field Programmable Gate Array (FPGA)	**03**
	(b)	Explain Successive Approximation type A/D converter.	**04**
	(c)	Give a brief on various types of memories.	**07**

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