Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER–IV (NEW) EXAMINATION – WINTER 2024

Subject Code:3140707 Date:22-11-2024

Subject Name:Computer Organization & Architecture

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Explain signed representation of integer in computer. Write $(-12)_{10}$ in binary with 8 – bits using following representations (i) Signed magnitude (ii) Signed 1's complement (iii) Signed 2's complement	**03**
	(b)	List all registers used in 'Basic Computer' including their symbolic name, size and functionality.	**04**
	(c)	Explain memory reference instructions of 'Basic Computer'.	**07**
Q.2	**(a)**	Draw block diagram for 4-bit adder – subtractor.	**03**
	(b)	Write an assembly language program to add 50 numbers using a loop.	**04**
	(c)	Explain register stack and memory stack organizations.	**07**
		OR	
	(c)	Write three address and two address instructions program for the following arithmetic expression. Discuss advantages and limitations of both types of programs. X = (A * B / C) + (D / E)	**07**
Q.3	**(a)**	List and explain conflicts that occur in an instruction pipeline.	**03**
	(b)	Briefly explain address sequencing in microprogrammed control unit.	**04**
	(c)	Differentiate RISC and CISC.	**07**
		OR	
Q.3	**(a)**	Write a short note on SIMD array processor.	**03**
	(b)	Explain Fetch subroutine of microprogrammed control.	**04**
	(c)	Explain addition and subtraction with signed magnitude data. Also list hardware required for the same.	**07**
Q.4	**(a)**	Explain any three addressing modes with suitable example.	**03**
	(b)	Differentiate isolated I/O and memory mapped I/O	**04**
	(c)	Explain associative, set-associative and direct mapping of cache memory.	**07**
		OR	
Q.4	**(a)**	Explain functionality of flags used in 'Basic Computer'.	**03**
	(b)	What is handshaking? Explain source initiated data transfer using handshaking with neat diagram.	**04**

	(c)	Write a short note on virtual memory.	**07**
Q.5	**(a)**	Differentiate static RAM and Dynamic RAM.	**03**
	(b)	Write a short note on daisy chain priority interrupt.	**04**
	(c)	Explain any three multiprocessor interconnection structures.	**07**

OR

Q.5	**(a)**	Differentiate tightly coupled and loosely coupled multiprocessor systems.	**03**
	(b)	Write a short note on content addressable memory.	**04**
	(c)	Discuss cache coherence problem and its solutions.	**07**

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