Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–IV (NEW) EXAMINATION – SUMMER 2024

Subject Code:3140707 Date:20-07-2024

Subject Name: Computer Organization & Architecture

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Define RTL. Give an example of register transfer of data through accumulator.	**03**
	(b)	Explain instruction formats with its types.	**04**
	(c)	Explain Instruction cycle with flowchart.	**07**
Q.2	**(a)**	Differentiate MRI and non-MRI.	**03**
	(b)	Explain Memory reference instructions.	**04**
	(c)	Explain micro programmed control organization in detail.	**07**
		OR	
	(c)	What is register stack? Explain push and pop micro-operations.	**07**
Q.3	**(a)**	Explain subroutine call and return with micro-operation.	**03**
	(b)	State the differences between register stack and memory stack.	**04**
	(c)	What is addressing modes? List and explain any five addressing modes by taking proper example(s).	**07**
		OR	
Q.3	**(a)**	Write a short note on memory interleaving.	**03**
	(b)	Explain Flynn's classification of computer.	**04**
	(c)	Explain pipelining technique. Draw the general structure of four segment pipeline.	**07**
Q.4	**(a)**	Explain the role of associative memory.	**03**
	(b)	Explain in brief about Cache memory and Virtual memory.	**04**
	(c)	Discuss associative mapping and direct mapping in organization of cache memory.	**07**
		OR	
Q.4	**(a)**	Explain Content Addressable Memory.	**03**
	(b)	Compare SRAM and DRAM.	**04**
	(c)	Explain paging and address translation with example.	**07**
Q.5	**(a)**	Compare tightly coupled and loosely coupled systems.	**03**
	(b)	Write a note on crossbar switch interconnection structure with block diagram	**04**
	(c)	Describe cache coherence problem and its solutions in detail.	**07**
		OR	
Q.5	**(a)**	Explain CLA, ISZ and CMA instruction.	**03**
	(b)	Draw and explain in brief flowchart for interrupt cycle.	**04**
	(c)	Explain first pass of an assembler with flowchart.	**07**

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