Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER–III (NEW) EXAMINATION – WINTER 2024

Subject Code: 3131102 Date: 29-11-2024

Subject Name: Digital System Design

Time: 10:30 AM TO 01:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed**.

			Marks
Q.1	(a)	Convert the decimal number 345.75 to base 4, base 5, and base 9.	**03**
	(b)	Prove that NOR Gate is a Universal Gate.	**04**
	(c)	Simplify the following Boolean function, F(a,b,c,d) = ∑m(1,3,5,7,12,13,14) using the Quine-McCluskey Tabular Method.	**07**
Q.2	(a)	State De Morgan's Laws and provide a proof for them.	**03**
	(b)	Obtain the truth table of the function: F = (x + y)(x′ + z).	**04**
	(c)	Minimize the logic function F(A, B, C, D) = ΠM(0, 1, 2, 5, 8, 9, 10, 13) using K-map and draw the logic circuit for the simplified function using NOR gates only.	**07**
		OR	
	(c)	What is a multiplexer? Explain the working of a 4-to-1 multiplexer with the help of a logic circuit diagram and a truth table.	**07**
Q.3	(a)	How does the race-around condition occur in JK flip-flops, and what techniques are used to avoid it?	**03**
	(b)	What are the characteristics of JK flip-flops that differentiate them from SR and D flip-flops?	**04**
	(c)	Design a half adder and derive the full adder using half adders.	**07**
		OR	
Q.3	(a)	Distinguish between combinational and sequential logic circuits.	**03**
	(b)	How can you implement a 4x16 decoder using two 2x4 decoders?	**04**
	(c)	Explain working of master-slave JK flip-flop with necessary logic diagram, state equation and state diagram.	**07**
Q.4	(a)	Explain the problem associate of an asynchronous state machine with the help of one example	**03**
	(b)	Draw logic diagram, graphical symbol and Characteristic table for clocked D flip-flop	**04**
	(c)	Draw and explain Ring counter	**07**
		OR	
Q.4	(a)	How many flip-flops are needed to design a counter that counts from 0 to 31? Explain your reasoning.	**03**
	(b)	What are the different classifications of logic families? Compare their characteristics.	**04**
	(c)	A combinational logic circuit is defined by the functions: F1= Σ (3, 5, 6, 7) and F2= Σ (0, 2, 4, 7). Implement the circuit with a PLA having three inputs, four product terms and two outputs.	**07**

Q.5	(a)	List the steps in VLSI Design flow.	**03**
	(b)	Describe a Moore machine.	**04**
	(c)	Design a synchronous BCD counter with JK flip-flops.	**07**

OR

Q.5	(a)	Define the following: 1. Fan-in 2. Noise Margin 3. Propagation Delay	**03**
	(b)	Describe the operation of a 4-bit parallel-in parallel-out shift register.	**04**
	(c)	Design a 3-bit synchronous counter using positive edge-triggered D flip-flops.	**07**

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