Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III (NEW) EXAMINATION – WINTER 2023

Subject Code:3131102 Date:18-01-2024

Subject Name:Digital System Design

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Briefly explain the steps for VLSI design flow.	**03**
	(b)	Implement Full Adder using 3×8 decoder.	**04**
	(c)	Design BCD to Excess-3 code converter.	**07**
Q.2	**(a)**	Explain NAND SR Latch.	**03**
	(b)	Reduce the following expression using K-map. Σ (2, 3, 6,7,8,10,11,14)	**04**
	(c)	Explain dual slope type A/D converter in detail.	**07**
		OR	
	(c)	Design 2-bit magnitude comparator.	**07**
Q.3	**(a)**	Compare synchronous and asynchronous counter.	**03**
	(b)	Obtain JK flip-flop from SR flip-flop.	**04**
	(c)	Design a 3-bit synchronous counter using JK flip-flop.	**07**
		OR	
Q.3	**(a)**	Compare TTL, ECL, & CMOS logic families.	**03**
	(b)	Discuss general state machine architecture.	**04**
	(c)	Design mod-6 asynchronous counter using T flip-flop.	**07**
Q.4	**(a)**	Compare asynchronous and synchronous state machines.	**03**
	(b)	Explain working of D flip-flop with characteristic table and logic diagram.	**04**
	(c)	Implement the following using MUX: a) $F(A,B,C) = \sum(1,3,6)$ b) $F(A,B,C) = \pi(2,3,5)$	**07**
		OR	
Q.4	**(a)**	Define Noise margin, Propagation delay, fan-in and fan-out	**03**
	(b)	State and prove De Morgan's theorem.	**04**
	(c)	Describe working principle of Programmable Logic Array with block diagrams.	**07**
Q.5	**(a)**	Explain half subtractor with logic circuit.	**03**
	(b)	Explain minterms and maxterms.	**04**
	(c)	Describe the operation of 4-bit bidirectional shift register with logic diagram.	**07**
		OR	
Q.5	**(a)**	Compare sequential and combinational circuits.	**03**
	(b)	Discuss working fundamentals behind FINFET.	**04**
	(c)	Explain Universal Gates.	**07**

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