Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III EXAMINATION – SUMMER 2025

Subject Code:3131102 Date:31-05-2025

Subject Name:Digital System Design

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Convert the decimal Number 250.5 to base 4 and base 8.	**03**
	(b)	State and prove DeMorgan's Theorem.	**04**
	(c)	Minimize the following function in SOP and POS minimal form using K-Maps: F(A, B, C, D) =∑m(1, 2, 6, 7, 8, 13, 14, 15) + d(3, 5, 12)	**07**
Q.2	**(a)**	Convert F(A,B,C) = BC+A into standard minterm form.	**03**
	(b)	Implement Ex -NOR and Ex-OR using NAND and NOR only.	**04**
	(c)	Implement the full adder & full subtractor using Multiplexer.	**07**
		OR	
	(c)	Design and implement binary to Excess-3 code converter.	**07**
Q.3	**(a)**	Obtain the truth table of the function: F = xy+yz+zx.	**03**
	(b)	Obtain JK flip-flop from SR flip-flop.	**04**
	(c)	Draw the circuit diagrams and truth table of SR, D, T and JK flip flops.	**07**
		OR	
Q.3	**(a)**	What is "Lock out" condition in counter? How to avoid it?	**03**
	(b)	Implement 4x16 decoder using two 3x8 decoder.	**04**
	(c)	Explain Master Slave JK flip-flop with truth table and circuit diagram.	**07**
Q.4	**(a)**	Compare sequential and combinational circuits.	**03**
	(b)	Define the following characteristics of IC: (i) Propagation Delay (ii) Figure of Merit (iii) Fan out (vi) Noise Margin	**04**
	(c)	Compare ROM, PLA and PAL.	**07**
		OR	
Q.4	**(a)**	Compare Latch and a Flip flop.	**03**
	(b)	Give classification of logic families and compare CMOS and TTL.	**04**
	(c)	Explain Moore machine.	**07**
Q.5	**(a)**	List the steps in VLSI Design flow.	**03**
	(b)	Design Modulo-8 counter using T flip flop.	**04**
	(c)	With neat sketch design 4-bit bidirectional shift register.	**07**
		OR	
Q.5	**(a)**	Define State Table and State Diagram.	**03**
	(b)	Design mod-6 asynchronous counter using T flip-flop.	**04**
	(c)	Design 4-bit ripple counter using negative edge triggered JK flip flop.	**07**

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