Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III (NEW) EXAMINATION – SUMMER 2024

Subject Code:3131102 Date:29-06-2024

Subject Name: Digital System Design

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Convert the decimal number 250.5 to base 3, base 7 and base 8.	**03**
	(b)	Show that NAND Gate is a Universal Gate.	**04**
	(c)	simplify the following Boolean function, F(w,x,y,z)=∑m(2,6,8,9,10,11,14,15) using Quine-McClukey tabular Method.	**07**
Q.2	**(a)**	Show that (A ⊕B ⊕C)' = (A ⊙B ⊙C).	**03**
	(b)	Obtain the truth table of the function: F= xy + xy′ + y′z.	**04**
	(c)	Minimize the logic function F (A,B,C,D)= Π_M(1, 2, 3, 8, 9, 10, 11,14) using K map & Draw the logic circuit for the simplified function using NOR gates only.	**07**
		OR	
	(c)	What is multiplexer? With logic circuit and function table explain the working of 4 to 1 line multiplexer.	**07**
Q.3	**(a)**	What is race around condition in JK flip flop?	**03**
	(b)	List out problems of asynchronous circuit. Also exemplify any two problems with suitable examples.	**04**
	(c)	With necessary sketch explain Bidirectional Shift Register with parallel load.	**07**
		OR	
Q.3	**(a)**	Implement 8x1 MUX using 4x1 MUX.	**03**
	(b)	Implement 4x16 decoder using two 3x8 decoder.	**04**
	(c)	Explain working of master-slave JK flip-flop with necessary logic diagram, state equation and state diagram.	**07**
Q.4	**(a)**	Define the terms 1. Fan out 2.Noise Margin 3. Fan in	**03**
	(b)	Design Modulo-8 counter using T flip flop.	**04**
	(c)	Explain Moore machine.	**07**
		OR	
Q.4	**(a)**	How many flip-flops are required to build a digital counter to count from 0 to 63? Justify.	**03**
	(b)	What are the classifications of Logic families? Also list the characteristics of digital IC.	**04**
	(c)	Compare ROM, PLA and PAL.	**07**
Q.5	**(a)**	List the steps in VLSI Design flow.	**03**
	(b)	Describe General State Machine Architecture with suitable diagrams.	**04**
	(c)	Design a synchronous BCD counter with JK flip-flops.	**07**
		OR	
Q.5	**(a)**	Implement T flip flop using D flip flop.	**03**
	(b)	Explain 4 bit serial in serial out shift register.	**04**
	(c)	Design 4-bit ripple counter using negative edge triggered JK flip flop.	**07**

****