GUJARAT TECHNOLOGICAL UNIVERSITY

BE-3 SEMESTER –OLD PAPER– W22 TO S25- QUESTION BANK

Subject Name & Code:

Analog and Digital Electronics- 3130907

Unit 1: Differential, Multi-stage and Operational Amplifiers

Repeated Questions:

1. **List/State all ideal characteristics of an op-amp.**
   - **(03 Marks)** - SUM 25 (Q1a), WIN 24 (Q3a), SUM 24 (Q1a)
   - **(07 Marks)** - WIN 22 (Q1c), SUM 23 (Q1c)
2. **Define/Describe: Slew Rate, Input Offset Voltage, Input Bias Current, Input Offset Current.**
   - **(03 Marks)** - SUM 25 (Q1b), WIN 24 (Q2a), WIN 22 (Q1a), SUM 23 (Q1a)
   - **(04 Marks)** - WIN 24 (Q2b)
3. **Draw the block diagram/internal structure of a typical Op-Amp and explain the function of each block.**
   - **(07 Marks)** - WIN 24 (Q2c), SUM 24 (Q1c), WIN 22 (Q1c), SUM 23 (Q1c)
4. **Draw the equivalent circuit of an Op-Amp and explain each part.**
   - **(07 Marks)** - WIN 23 (Q1c)
5. **What is cross-over distortion in a power amplifier?**
   - **(04 Marks)** - WIN 23 (Q1b), SUM 23 (Q1b)

Other Important Questions:

1. **Explain the ideal voltage transfer characteristics of an Op-Amp. (04 Marks)** - WIN 22 (Q1b)
2. **Explain the procedure of offset voltage compensation / use of external offset voltage compensation circuits in an op-amp. (03/04 Marks)** - WIN 22 (Q2a), SUM 24 (Q3b)
3. **Draw a transistor C-E amplifier circuit. Draw its AC equivalent circuit. (03 Marks)** - WIN 23 (Q1a)
4. **Numerical:** A non-inverting op-amp with R1=1kΩ and RF=10kΩ has parameters: A=200,000, Ri=2MΩ, Ro=75Ω, fo=5Hz, Supply voltages = ±15V, Output Voltage Swing = ±13V. Find the values of AF,RIF,RoF. **(07 Marks)** - SUM 25 (Q3b) *[This is a crucial numerical problem from the closed-loop chapter but is based on internal op-amp parameters. Practice this.]*

Unit 2: Linear Applications of Op-Amp

Repeated Questions:

1. **Explain the working of an Op-Amp as an Integrator with circuit, waveform, and derivation.**
   - **(07 Marks)** - SUM 25 (Q2c-OR), WIN 24 (Q3b), SUM 24 (Q2c), WIN 22 (Q2c-OR)
2. **Explain the working of an Instrumentation Amplifier. List its advantages and applications.**
   - **(07 Marks)** - SUM 25 (Q3c), WIN 24 (Q3b-OR), WIN 23 (Q2a)
3. **Explain the working of a Voltage Follower circuit. State its applications.**
   - **(03 Marks)** - SUM 25 (Q3a-OR), WIN 22 (Q2b)
4. **Draw and explain the working of a Summing Amplifier. (07 Marks)** - WIN 24 (Q3c-OR)
5. **Draw and explain the working of an Inverting Amplifier. Derive its gain. (07 Marks)** - WIN 24 (Q3c), SUM 25 (Q3c-OR)
6. **Draw and explain the working of a Differential Amplifier. (07 Marks)** - WIN 24 (Q2c-OR)
7. **Discuss the classification of active filters and explain the frequency response of each type. (07 Marks)** - WIN 23 (Q2c)
8. **Compare RC phase shift and Wien bridge oscillator. (03 Marks)** - SUM 25 (Q3a), SUM 23 (Q5a)
9. **Sketch and explain the Wien bridge oscillator. (04 Marks)** - WIN 23 (Q3b)
10. **Design an R-C phase shift oscillator for a given frequency. (04 Marks)** - SUM 23 (Q2b) *[Numerical Problem]*

Other Important Questions:

1. **Explain Op-Amp as a phase shift amplifier. (03 Marks)** - WIN 24 (Q3a-OR)
2. **Discuss (i) CMRR (ii) Slew Rate (07 Marks)** - SUM 25 (Q2c)
3. **Prove that the voltage follower has unity gain. (04 Marks)** - WIN 23 (Q2b)
4. **Numerical:** For an inverting amplifier, V1=1V, V2=3V, V3=2V with R1=R2=R3=2KΩ and RF=3KΩ. Determine Vout. **(03 Marks)** - SUM 23 (Q3a) *[Numerical Problem]*

Unit 3: Nonlinear Applications of Op-Amp

Repeated Questions:

1. **Draw and explain the working of a Zero Crossing Detector with waveforms and applications.**
   - **(07 Marks)** - SUM 25 (Q2a), WIN 24 (Q1c)
   - **(04 Marks)** - SUM 24 (Q3b-OR), WIN 23 (Q3c)
2. **Draw and explain the working of a Precision Rectifier.**
   - **(04 Marks)** - WIN 24 (Q4b-OR), WIN 23 (Q3b-OR)
3. **Explain how to generate a Triangular wave using an Op-Amp.**
   - **(04 Marks)** - SUM 24 (Q2b), WIN 23 (Q3a-OR)
4. **Explain the working of a Peak Detector (Positive/Negative).**
   - **(07 Marks)** - SUM 24 (Q2c-OR), SUM 23 (Q3c)
   - **(04 Marks)** - WIN 24 (Q4b), WIN 23 (Q3a)
5. **Compare a Comparator and a Schmitt Trigger circuit. (04 Marks)** - SUM 25 (Q3b-OR)
6. **Draw a Schmitt trigger circuit. Plot input and output waveforms. (04 Marks)** - SUM 23 (Q5b)

Other Important Questions:

1. **Write a short note on P, PI, and PID controllers using an op-amp.** *[From Syllabus, not directly asked but important concept]*

Unit 4: Combinational Digital Circuits

Repeated Questions:

1. **Minimize a given Boolean expression using K-Map (with/without don't care conditions).**
   - **(07 Marks)** - SUM 25 (Q4c), WIN 22 (Q3b), WIN 23 (Q4c), SUM 23 (Q4c-OR)
   - **(04 Marks)** - SUM 24 (Q4b-OR)
2. **Implement a logic function using an 8:1 Multiplexer (MUX).**
   - **(04 Marks)** - SUM 24 (Q4c), WIN 22 (Q3a), SUM 23 (Q3b)
3. **Compare Combinational and Sequential circuits.**
   - **(03 Marks)** - SUM 25 (Q4a), WIN 24 (Q4a), WIN 23 (Q5b), WIN 22 (Q4a-OR)
4. **Compare Decoder and Demultiplexer. (03 Marks)** - SUM 24 (Q4a)
5. **Explain/Design a Full Adder circuit.**
   - **(04 Marks)** - WIN 23 (Q4b)
   - **(07 Marks)** - SUM 23 (Q4c-OR)
6. **Explain/Design a Full Subtractor circuit.**
   - **(07 Marks)** - WIN 24 (Q4c-OR), WIN 22 (Q3c-OR)
   - **(04 Marks)** - SUM 24 (Q4c-OR)
7. **State and explain don't care conditions in K-Map with an example. (07 Marks)** - WIN 24 (Q4c)
8. **Describe a 3 to 8 line decoder with a logic diagram and truth table. (07 Marks)** - SUM 24 (Q3c-OR)
9. **Design a decimal to binary encoder. (04 Marks)** - SUM 25 (Q4b-OR)

Other Important Questions:

1. **Reduce a function using Boolean Algebra laws. (03 Marks)** - SUM 24 (Q3a-OR)
2. **Implement a full adder using a multiplexer. (07 Marks)** - SUM 24 (Q4c)
3. **Write a short note on binary codes / Gray code. (04 Marks)** - WIN 23 (Q4b), SUM 23 (Q4b-OR)
4. **Define a 3-bit parity generator circuit. (04 Marks)** - WIN 22 (Q5b)
5. **List the steps of the Quine-McCluskey method. (03 Marks)** - SUM 25 (Q4a-OR) *[Rarely asked but in syllabus]*

Unit 5: Sequential Circuits and Systems

Repeated Questions:

1. **Explain the working of a Master-Slave J-K Flip Flop with a diagram.**
   - **(07 Marks)** - SUM 25 (Q1c), WIN 24 (Q4c), WIN 22 (Q4c), SUM 23 (Q4b)
2. **Explain the working of an S-R / J-K / D Flip Flop.**
   - **(07 Marks)** - WIN 24 (Q5b-OR), WIN 22 (Q4c-OR), SUM 23 (Q2c-OR)
3. **Differentiate between Asynchronous and Synchronous counters.**
   - **(04 Marks)** - SUM 24 (Q4a-OR), WIN 22 (Q5b)
   - **(07 Marks)** - WIN 24 (Q5c)
4. **State the applications of Shift Registers.**
   - **(03 Marks)** - SUM 25 (Q4b), WIN 24 (Q5a)
5. **Explain/Draw a 4-bit Bidirectional Shift Register. (04 Marks)** - SUM 24 (Q4b)
6. **Write a note on Ring Counter. (07 Marks)** - SUM 25 (Q4c-OR)
7. **What are Preset and Clear inputs? Why are they used? (03 Marks)** - WIN 22 (Q4a)
8. **Differentiate between a latch and a flip-flop. (03 Marks)** - WIN 24 (Q4a-OR)
9. **Design a 4-bit synchronous up counter. (07 Marks)** - WIN 23 (Q5c)
10. **Design a D FF using an SR FF. (03 Marks)** - SUM 23 (Q4a-OR)

Other Important Questions:

1. **Explain the different types of triggering methods for flip-flops. (03 Marks)** - WIN 23 (Q4a)
2. **Classify the various modes of operation of a shift register. (04 Marks)** - WIN 22 (Q4b)
3. **Write a short note on Parallel-In-Serial-Out (PISO) shift register. (04 Marks)** - WIN 22 (Q4b-OR)
4. **Explain memory and differentiate between 1-bit and 1-byte memory. (03 Marks)** - WIN 24 (Q1a)

Unit 6: A/D and D/A Converters

Repeated Questions:

1. **Explain the working of an R-2R Ladder D/A Converter with a diagram and necessary equations.**
   - **(07 Marks)** - SUM 25 (Q5c), SUM 24 (Q5b), WIN 22 (Q5c), SUM 23 (Q5b)
   - **(04 Marks)** - WIN 23 (Q5b-OR)
2. **Explain the working of a Successive Approximation A/D Converter.**
   - **(07 Marks)** - WIN 24 (Q5c-OR), SUM 24 (Q5c), WIN 22 (Q5c)
3. **Define/Discuss the following specifications for DAC: Accuracy, Resolution, Settling Time.**
   - **(03 Marks)** - SUM 25 (Q5a), WIN 23 (Q5a), SUM 24 (Q5a-OR)
4. **Define/Discuss the following specifications for ADC: Resolution, Conversion Time, Quantization Error.**
   - **(03 Marks)** - SUM 24 (Q5a), WIN 22 (Q5a)
   - **(04 Marks)** - SUM 25 (Q5b)
5. **Explain a Sample and Hold circuit.**
   - **(03 Marks)** - WIN 24 (Q5a-OR), WIN 23 (Q5a-OR)
6. **Explain the Parallel Comparator (Flash) A/D converter. (04 Marks)** - WIN 24 (Q5b)
7. **List/Illustrate different methods (types) of A/D conversion. (04 Marks)** - WIN 23 (Q5b-OR)

Other Important Questions:

1. **Numerical:** What will be the resolution of a 4-bit ADC with a 5V input? Define quantization error. **(04 Marks)** - SUM 24 (Q5b-OR) *[Important Numerical]*
2. **Explain a D/A converter with binary-weighted resistors. (07 Marks)** - SUM 24 (Q5c)
3. **Draw & explain a Flash A/D converter. Mention its pros and cons. (07 Marks)** - SUM 23 (Q5c)
4. **Explain a dual-slope A/D converter.** *[From Syllabus, not heavily asked but important]*

Summary of High-Weightage, Must-Prepare Topics:

- **Op-Amp Characteristics (Ideal & Non-Ideal):** Definitions and block diagram are extremely frequent.
- **Linear Op-Amp Circuits:** Integrator, Inverting Amp, Instrumentation Amp are guaranteed.
- **K-Map Minimization:** A sure 7-mark question.
- **Multiplexer/Demultiplexer/Decoder Implementation:** Very common.
- **Flip-Flops (JK Master-Slave is favorite):** Theory and applications.
- **D/A Converter (R-2R Ladder):** The most asked DAC question.
- **A/D Converter (Successive Approximation):** The most asked ADC question.
- **Specifications of DAC/ADC:** Definitions are frequently asked for 3 marks.

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