GUJARAT TECHNOLOGICAL UNIVERSITY

BE 5 SEMESTER – OLD PAPER – S22 TO S26 – QUESTION BANK

Subject Name & Code: VLSI Design - 3151105

Chapter 1: Introduction

Repeated Questions:

1. VLSI Design Styles:

- **Q.** Explain the impact of full-custom and semi-custom VLSI design style on design cycle time and circuit performance. **(WINTER 2022, 4 Marks; SUMMER 2023, 7 Marks; WINTER 2025, 4 Marks)**
- **Q.** Compare Full custom, Semi-custom and Fully Programmable VLSI design style. **(SUMMER 2024, 3 Marks; WINTER 2024, 3 Marks; SUMMER 2026, 3 Marks)**

2. Design Principles and Design Flow:

- **Q.** Define concepts of Regularity, Modularity and Locality. **(SUMMER 2022, 3 Marks; SUMMER 2024, 4 Marks; SUMMER 2026, 4 Marks)**
- **Q.** Draw and explain VLSI design flow Y chart. **(WINTER 2023, 7 Marks OR; WINTER 2024, 3 Marks; SUMMER 2026, 3 Marks)**

3. Chip Reliability:

- **Q.** What is chip reliability? List the four major causes for chip reliability problems. **(WINTER 2022, 3 Marks; WINTER 2025, 3 Marks)**

Other Important Questions:

1. Fabrication and Programmable Devices (Theory):

- **Q.** What is the role of photo resist material in IC fabrication process? **(SUMMER 2023, 3 Marks)**
- **Q.** Explain in short: FPGA. **(SUMMER 2022, 3 Marks)**

Chapter 2: Fabrication of MOSFET

Repeated Questions:

1. Fabrication Process Steps:

- **Q.** Explain process steps for fabrication of n-type MOSFET. **(SUMMER 2022, 7 Marks; WINTER 2022, 7 Marks; SUMMER 2025, 4 Marks; SUMMER 2026, 7 Marks)**
- **Q.** Write down basic steps of Local oxidation of Silicon (LOCOS) process. **(SUMMER 2023, 7 Marks; WINTER 2025, 7 Marks)**

2. Lithography:

- **Q.** Describe usage of photo resist in lithography process. Differentiate positive and negative photo resist material. **(WINTER 2023, 4 Marks; WINTER 2024, 4 Marks)**

Other Important Questions:

1. CMOS Fabrication and Device Isolation (Theory):

- **Q.** Draw and explain various fabrication steps for CMOS inverter with proper notations at each fabrication steps. **(SUMMER 2024, 7 Marks)**
- **Q.** Which material is used for gate formation of CMOS transistor? What is feature size? Among BJT and MOS which device is smaller in size? **(WINTER 2023, 3 Marks)**
- **Q.** Present device isolation techniques in fabrication process. **(SUMMER 2025, 3 Marks)**

Chapter 3: MOS Transistor

Repeated Questions:

1. MOS Structure and Threshold Voltage (Theory):

- **Q.** Explain the MOS system under external bias for accumulation, depletion and inversion regions. **(SUMMER 2022, 4 Marks; WINTER 2022, 7 Marks; SUMMER 2025, 4 Marks; WINTER 2025, 7 Marks)**
- **Q.** Derive threshold voltage equation of MOSFET. **(WINTER 2024, 7 Marks; SUMMER 2026, 7 Marks)**
- **Q.** What is substrate bias effect? Explain its analysis. **(WINTER 2022, 4 Marks; SUMMER 2023, 4 Marks OR; WINTER 2024, 7 Marks; SUMMER 2025, 3 Marks OR; WINTER 2025, 3 Marks)**

2. Drain Current and Channel Length Modulation (Theory):

- **Q.** Derive the drain current equation for MOSFET using Gradual Channel Approximation (GCA). **(SUMMER 2022, 7 Marks; WINTER 2022, 7 Marks OR; SUMMER 2024, 4 Marks; WINTER 2024, 7 Marks; SUMMER 2026, 7 Marks OR)**
- **Q.** What is channel length modulation? How it affects drain current of MOSFET? **(WINTER 2022, 4 Marks; SUMMER 2023, 7 Marks OR; WINTER 2025, 4 Marks)**

3. Scaling and Small-Geometry Effects (Theory):

- **Q.** Compare constant voltage scaling and constant field scaling. **(SUMMER 2023, 3 Marks; WINTER 2024, 3 Marks; SUMMER 2026, 4 Marks)**
- **Q.** Explain two types of scaling with its advantages and disadvantages. **(WINTER 2023, 7 Marks; WINTER 2024, 3 Marks)**
- **Q.** List/Enlist MOSFET scaling and small-geometry effects. What is hot carrier effect and punch through in small geometries devices? **(SUMMER 2023, 4 Marks; SUMMER 2025, 3 Marks)**

4. Numerical:

- **Q.** Consider a p-channel MOSFET with parameters $\mu p = 300\ cm^2/V\text{-}s$, $Cox = 6.9 \times 10^{-8}\ F/cm^2$, (W/L) = 10, and VTP = -0.65 V. Determine the maximum current at VGS = -3 V. **(WINTER 2023, 3 Marks)**

Other Important Questions:

1. MOS Structure and Capacitances (Theory):

- **Q.** Note down physical parameters affecting the threshold voltage of MOS structure. **(SUMMER 2023, 4 Marks)**
- **Q.** Explain the junction capacitances associated with MOS structure. Explain MOSFET capacitance in brief. **(SUMMER 2023, 7 Marks; SUMMER 2024, 3 Marks)**
- **Q.** For MOS structure, derive the expression for the maximum possible depth of the depletion region. **(WINTER 2023, 4 Marks)**

2. Current-Voltage Characteristics (Theory):

- **Q.** Draw cross section of n-channel MOSFET. Obtain drain current expression as a function of VGS, VDS, and VBS for linear and saturation region of operation of MOSFET device. **(WINTER 2023, 7 Marks)**
- **Q.** Write the equations describing the current-voltage characteristics of MOSFET. **(SUMMER 2025, 3 Marks)**
- **Q.** Identify following statements are True or False. Make correction if false and justify. (i) NMOS is constructed on n type and PMOS is constructed on p type substrate. (ii) If substrate is connected with VDD then threshold voltage VT = VT0 (iii) If VDS is constant and VGS increases then current IDS in NMOS transistor will increase. **(WINTER 2023, 3 Marks)**
- **Q.** Define and explain DIBL. **(SUMMER 2025, 3 Marks)**

3. Numerical:

- **Q.** Find the depletion layer width, depletion region charge and threshold voltage with no substrate bias with the following physical parameters. VSB = 0, for silicon gate n channel MOS transistor, with the following parameters: Substrate doping density NA = 1.5×10^{16} cm^{-3}, Gate donor doping ND = 10^{18} cm^{-3}, Gate oxide thickness tox = 400 Å, Nss = 10×10^{10} cm^{-3}. Consider Boltzmann Constant = 1.38×10^{-23} (J/K), Electron charge = 1.6×10^{-19} C, Intrinsic Silicon carrier concentration ni = 1.45×10^{10} cm^{-3}, εSi = 1.035×10^{-12} F/cm, $\varepsilon_o = 8.85 \times 10^{-14}$ F/cm, εox = 0.345×10^{-12} F/cm. **(SUMMER 2024, 7 Marks)**
- **Q.** For an enhancement type NMOS transistor has its source terminal connected to ground and 3 V connected to the gate. NMOS has VT = 2 V, λ = 0.04 1/V, μn·Cox = 20 A/V^2, W = 200 μm and L = 10 μm, VG = 3 V, VD = 0.5 V and 1 V. Calculate Drain Current ID. **(SUMMER 2024, 7 Marks OR)**
- **Q.** Consider reverse biased abrupt silicon p-n junction. The doping density of the n-type region is ND = 10^{19} cm^{-3} and the doping density of the p-type region is given as NA = 10^{16} cm^{-3}. The junction area is A = 20 μm × 20 μm. Calculate the built-in junction potential and zero bias junction capacitance per unit area for the structure. **(WINTER 2023, 7 Marks)**
- **Q.** Calculate the threshold voltage VTO and substrate bias coefficient at VSB = 0, for silicon gate n-channel MOS transistor, with the following parameters: substrate doping density NA = 3×10^{16} cm^{-3}, ND = 4×10^{19} cm^{-3}, gate oxide thickness tox = 200 Å, and oxide interface fixed charge density Nox = 10^{10} cm^{-2}. Assume ϕF(gate) = 0.56 V. **(WINTER 2023, 7 Marks OR)**
- **Q.** Measured voltage and current data for a MOSFET are given below: Determine the type of the device and calculate the parameters kn, VTO, and γ. Assume ϕF = -0.3 V. Assume MOSFET is enhancement type and neglect channel length modulation effect. [Diagram required – refer to the original question paper] **(SUMMER 2022, 7 Marks OR)**

Chapter 4: MOS Inverters - Static Characteristics

Repeated Questions:

1. VTC, Critical Voltages and Noise Margin (Theory):

- **Q.** Draw VTC of practical Inverter and define all critical voltages (VIL, VIH, VOL, VOH, NML, NMH). **(SUMMER 2022, 3 Marks OR; SUMMER 2024, 3 Marks OR; WINTER 2024, 4 Marks; SUMMER 2026, 3 Marks)**
- **Q.** Explain noise margin. **(SUMMER 2022, 3 Marks)**
- **Q.** Explain: Body effect and Noise margin. **(SUMMER 2023, 4 Marks OR)**

2. Resistive Load Inverter (Theory):

- **Q.** Draw resistive load inverter. Derive VIL and VIH critical voltages equation of resistive load inverter. **(WINTER 2023, 7 Marks OR; WINTER 2024, 4 Marks; SUMMER 2026, 4 Marks)**
- **Q.** Draw the VTC of resistive load inverter circuit and show the 3 different operating regions of MOSFET of the circuit on it. **(WINTER 2022, 3 Marks)**
- **Q.** Present the analysis of the resistive load inverter. Derive critical voltages and noise margins. **(SUMMER 2025, 7 Marks)**

3. Depletion Load nMOS Inverter and Inverter Comparison (Theory):

- **Q.** Draw the inverter circuit with depletion type nMOS load. Mention the operating regions of driver and load transistors for different input voltages. Derive critical voltage points VOH, VOL, VIH and VIL for depletion-load nMOS inverter. **(SUMMER 2024, 4 Marks OR; WINTER 2025, 4 Marks)**
- **Q.** Give the comparison of resistive load, depletion load and CMOS inverter circuits. **(SUMMER 2023, 7 Marks OR)**

4. CMOS Inverter (Theory):

- **Q.** Derive VIL and VIH critical voltage equations for CMOS inverter. **(SUMMER 2022, 7 Marks OR; WINTER 2022, 7 Marks; WINTER 2024, 4 Marks OR; SUMMER 2026, 4 Marks OR)**
- **Q.** Derive expression of threshold voltage for CMOS inverter. **(WINTER 2023, 4 Marks)**
- **Q.** Why in symmetrical and ideal CMOS inverter required $(W/L)p \approx 2.5\ (W/L)n$? Explain in detail. **(WINTER 2025, 4 Marks OR)**

5. Numerical:

- **Q.** Consider a resistive load inverter circuit with VDD = 5 V, Kn' = 10 µA/V², VTO = 0.8 V, RL = 400 kΩ and W/L = 2. Calculate the critical Voltages (VOH, VOL, VIL and VIH) on the VTC and find the noise margins of the circuit. **(SUMMER 2022, 7 Marks; SUMMER 2024, 7 Marks)**
- **Q.** Consider a CMOS inverter with the following parameters: VDD = 3.3 V, VTON = 0.6 V, VTOP = -0.7 V, kn = 200 µA/V² and kp = 160 µA/V² (or 80 µA/V²). Calculate the noise margins of the circuit. **(WINTER 2022, 7 Marks OR; SUMMER 2024, 7 Marks OR; WINTER 2024, 7 Marks OR; WINTER 2025, 7 Marks; SUMMER 2026, 7 Marks OR - parameters vary slightly across papers)**

Other Important Questions:

1. Numerical:

- **Q.** Consider a resistive-load inverter with RL = 200 kΩ. The enhancement-type nMOS driver transistor has the following parameters VDD = 5 V, VTO = 0.8 V, µnCox = 20 µA/V², W/L = 2. Determine VOL, VIL and NML. **(WINTER 2024, 7 Marks)**
- **Q.** Consider a resistive load inverter circuit with VDD = 5 V, k'n = 20 µA/V², VTO = 0.8 V, RL = 200 kΩ and W/L = 2. Calculate VOL and VIH on the VTC of the inverter. **(WINTER 2025, 7 Marks OR)**
- **Q.** Consider a resistive-load inverter circuit with VDD = 5 V, kn' = 20 µA/V², VT0 = 0.8 V, RL = 200 kΩ, and W/L = 2. Find noise margin high NMH. **(SUMMER 2026, 7 Marks)**

Chapter 5: MOS Inverters Switching characteristics and Interconnect Effects

Repeated Questions:

1. Propagation Delay and Power Dissipation:

- **Q.** Define propagation delay, Rise time and Fall time. **(SUMMER 2022, 3 Marks; SUMMER 2023, 3 Marks; SUMMER 2025, 4 Marks)**
- **Q.** Derive the equation for propagation delay of output signal during high to low transition (τpHL) of output of CMOS inverter circuit with Cload as load capacitance. **(SUMMER 2022, 4 Marks OR; WINTER 2022, 7 Marks; SUMMER 2024, 4 Marks; WINTER 2024, 7 Marks; WINTER 2025, 7 Marks OR; SUMMER 2026, 7 Marks)**
- **Q.** In CMOS inverter circuit, define propagation delay TPLH (low-to-high transition at output) and obtain its expression. **(SUMMER 2023, 7 Marks)**
- **Q.** Explain switching power dissipation of CMOS inverter. **(WINTER 2023, 4 Marks OR; SUMMER 2025, 4 Marks OR; WINTER 2025, 4 Marks; SUMMER 2026, 7 Marks OR)**
- **Q.** What is meant by static and dynamic power dissipation? **(SUMMER 2024, 3 Marks)**
- **Q.** Present timing analysis of CMOS inverter. **(SUMMER 2025, 7 Marks)**

2. Ring Oscillator:

- **Q.** Draw three stage CMOS ring oscillator circuit with necessary waveforms. Write generated frequency equation. **(SUMMER 2022, 7 Marks OR; SUMMER 2023, 3 Marks OR; SUMMER 2024, 3 Marks OR; WINTER 2024, 3 Marks OR; SUMMER 2026, 3 Marks)**
- **Q.** Draw diagram of ring oscillator. For five stage ring oscillator circuit, derive expression for frequency of oscillation. **(WINTER 2023, 4 Marks)**

3. Interconnect Effects:

- **Q.** Illustrate the RC delay models for calculation of interconnect delay. Explain Elmore delay with suitable diagram. **(SUMMER 2022, 7 Marks; WINTER 2022, 4 Marks; WINTER 2024, 7 Marks OR; WINTER 2025, 3 Marks)**
- **Q.** Discuss methods to estimate interconnect parasitic. **(WINTER 2023, 3 Marks OR)**

Other Important Questions:

None identified.

Chapter 6: Combinational MOS Logic Circuits

Repeated Questions:

1. Euler Path and Stick Diagram:

- **Q.** Explain the Euler path approach to find the optimized stick-diagram for any CMOS logic circuit. Draw the optimized stick-diagram for the following Boolean function (CMOS Logic), F = (A(D+E)+BC)'. **(WINTER 2023, 4 Marks OR; SUMMER 2024, 7 Marks; SUMMER 2024, 3 Marks OR; WINTER 2024, 3 Marks)**

2. Pass Transistor Logic and Transmission Gates:

- **Q.** Explain basic principles of Pass transistor circuits. How logic "1" transfer happens in nMOS pass transistor circuits. Explain with suitable example. **(SUMMER 2023, 4 Marks OR; SUMMER 2025, 3 Marks; WINTER 2025, 7 Marks)**
- **Q.** Explain the importance of CMOS Transmission gate? Draw 2×1 MUX using compound gate and compare it with 2×1 MUX based on transmission gate. Also draw 4×1 MUX based on transmission gate. **(SUMMER 2022, 4 Marks; WINTER 2023, 7 Marks; WINTER 2024, 7 Marks OR)**
- **Q.** Show with the diagram, bias conditions and operating regions of CMOS transmission gate, as a function of output voltage. **(SUMMER 2023, 4 Marks)**
- **Q.** Draw and explain the operation of two input multiplexer using CMOS transmission gates. **(WINTER 2022, 4 Marks)**
- **Q.** Realize following Boolean logic equation using Transmission Gate (TG). F = XY + X'Z' + XY'Z. **(WINTER 2024, 4 Marks; SUMMER 2026, 4 Marks)**
- **Q.** Analyze transmission gates (TGs) in detail. Also, describe the procedure for circuit design with TGs. **(SUMMER 2025, 7 Marks OR)**

3. XOR Realizations:

- **Q.** Realize XOR function using CMOS transmission gate. **(SUMMER 2022, 4 Marks OR; SUMMER 2023, 3 Marks; WINTER 2023, 3 Marks OR; WINTER 2025, 4 Marks OR)**
- **Q.** Draw CMOS implementation of XOR function. **(SUMMER 2022, 4 Marks OR)**
- **Q.** For the Exclusive OR function, draw with following realization 1. Static CMOS realization 2. Pseudo nMOS gate 3. CMOS Transmission Gate (TG). **(SUMMER 2024, 7 Marks OR)**

4. NAND Gate:

- **Q.** Draw CMOS circuit for NAND gate and derive threshold voltage equation for it. **(SUMMER 2023, 7 Marks OR; WINTER 2025, 3 Marks OR)**

Other Important Questions:

1. Pass Transistor Circuits (Numerical):

- **Q.** Two nMOS transistors (M1 and M2) connected in series is shown in Figure 1. The power supply is VDD = 3.3 V and the nMOS threshold VTN = 0.55 V. Find the output voltage at node b. Consider i) Va = 2.7 V and ii) Va = 3 V. [Diagram required – refer to the original question paper] **(SUMMER 2024, 4 Marks)**

2. Static CMOS Gates (Theory):

- **Q.** For the function Z = (A(D + E) + BC) / (D + E). Construct dual pull up graph from pull down graph using Dual Graph Concept. **(WINTER 2022, 4 Marks OR)**
- **Q.** Draw 2 input NAND gate using complementary pass transistor logic. **(WINTER 2023, 4 Marks)**
- **Q.** Explain two input CMOS NOR gate. **(SUMMER 2022, 4 Marks)**
- **Q.** Design 2-input OR, AND and XOR gate using CMOS. **(SUMMER 2025, 4 Marks)**
- **Q.** Explain AOI (AND-OR-INVERT) and OAI (OR-AND-INVERT) circuit categories with example for CMOS logic. **(WINTER 2025, 3 Marks)**

Chapter 7: Sequential MOS Logic Circuits

Repeated Questions:

1. Latches:

- **Q.** Draw CMOS implementation of D latch with two inverters and two CMOS TG gates. **(SUMMER 2022, 4 Marks OR; SUMMER 2023, 3 Marks OR; WINTER 2024, 4 Marks OR; WINTER 2025, 3 Marks; SUMMER 2026, 4 Marks OR)**
- **Q.** Design CMOS SR latch circuit based on NOR gate. Draw and explain 'clocked NOR based SR latch' with gate level circuit and waveform. **(SUMMER 2022, 4 Marks; WINTER 2022, 7 Marks OR; WINTER 2024, 4 Marks)**
- **Q.** Describe the behavior of bistable elements. Describe the operating principle of the SR latch circuit with the necessary diagrams. **(SUMMER 2025, 4 Marks OR; SUMMER 2025, 4 Marks OR)**
- **Q.** Draw transistor level circuit diagram of NAND based SR latch using CMOS. **(SUMMER 2024, 4 Marks)**

2. Flip-Flops:

- **Q.** Draw CMOS negative edge triggered master slave D flip flop and explain its working with proper circuit diagram. **(WINTER 2023, 7 Marks OR)**

3. Testability Concepts:

- **Q.** Explain controllability and Observability. **(SUMMER 2022, 3 Marks; WINTER 2022, 4 Marks OR; SUMMER 2023, 4 Marks OR; WINTER 2024, 3 Marks; WINTER 2025, 4 Marks; SUMMER 2026, 3 Marks OR - also mapped to Chapter 10, but appears in sequential context often)**

Other Important Questions:

1. Latches and Flip-Flops:

- **Q.** Implement and Describe CMOS clocked SR flip-flop. **(SUMMER 2024, 4 Marks OR)**
- **Q.** Describe the working of edge-triggered flip-flops with necessary diagrams. **(SUMMER 2025, 7 Marks)**
- **Q.** Draw the circuit of dynamic D-latch. **(WINTER 2022, 3 Marks OR)**
- **Q.** Draw the AOI based implementation of the clocked NOR based SR latch circuit. **(WINTER 2025, 3 Marks OR)**
- **Q.** Implement clocked JK latch using CMOS inverter. **(SUMMER 2026, 3 Marks OR)**

Chapter 8: Dynamic Logic Circuits

Repeated Questions:

1. Dynamic CMOS Logic:

- **Q.** How pre-charge and evaluate logic works for dynamic CMOS circuit? Explain with example. **(WINTER 2022, 7 Marks; WINTER 2025, 7 Marks)**
- **Q.** Explain Domino CMOS logic. **(SUMMER 2022, 7 Marks; WINTER 2024, 3 Marks OR; SUMMER 2026, 3 Marks OR)**
- **Q.** Differentiate the ratioed and ratio less dynamic logic circuits with examples. **(SUMMER 2023, 7 Marks)**

2. Voltage Bootstrapping:

- **Q.** Explain voltage bootstrapping. Derive the mathematical expression for dynamic Voltage bootstrapping circuit. **(SUMMER 2022, 7 Marks OR; WINTER 2023, 4 Marks OR; WINTER 2024, 7 Marks; SUMMER 2025, 7 Marks OR)**

Other Important Questions:

1. Dynamic Logic Techniques (Theory):

- **Q.** Explain cascading problem in dynamic CMOS logic. **(SUMMER 2023, 3 Marks)**
- **Q.** Draw and explain the basic circuit architecture of Zipper CMOS circuits with clock signals. **(SUMMER 2023, 4 Marks)**
- **Q.** Explain NORA CMOS logic and its advantages. **(WINTER 2022, 7 Marks OR)**
- **Q.** What are the limitations of Dynamic circuits? Discuss the effect of charge sharing and charge leakage in dynamic pass transistor logic. **(SUMMER 2024, 3 Marks)**
- **Q.** Discuss synchronous dynamic circuit techniques. **(SUMMER 2025, 4 Marks)**

Chapter 9: Chip I/P and O/P Circuits

Repeated Questions:

1. Latch-up:

- **Q.** What is latch up in CMOS circuits and how it can be prevented? Explain the factors behind latch-up problems. **(SUMMER 2022, 3 Marks OR; WINTER 2022, 3 Marks OR; SUMMER 2023, 7 Marks OR; SUMMER 2025, 7 Marks; SUMMER 2026, 4 Marks OR)**

2. Clocking:

- **Q.** What is clock-skew? Explain on-chip clock generation and distribution. **(SUMMER 2024, 7 Marks; WINTER 2024, 4 Marks OR; SUMMER 2026, 7 Marks)**
- **Q.** Elaborate different clock distribution network. **(WINTER 2022, 3 Marks)**
- **Q.** Present the analysis of on-chip clock generation and distribution techniques. **(SUMMER 2025, 7 Marks OR; WINTER 2025, 7 Marks OR)**

Other Important Questions:

1. Packaging (Theory):

- **Q.** List packaging technology used for VLSI chips. **(WINTER 2023, 3 Marks OR)**

Chapter 10: Design for testability

Repeated Questions:

1. Testability Concepts and Faults:

- **Q.** Explain controllability and observability. **(SUMMER 2022, 3 Marks; WINTER 2022, 4 Marks OR; SUMMER 2023, 4 Marks OR; WINTER 2024, 3 Marks; WINTER 2025, 4 Marks; SUMMER 2026, 3 Marks OR)**
- **Q.** Give examples of physical defects. List examples of physical defects during chip fabrication. **(SUMMER 2023, 3 Marks OR; WINTER 2023, 3 Marks)**
- **Q.** Discuss fault types and models. **(SUMMER 2022, 3 Marks; SUMMER 2025, 7 Marks)**

2. DFT and BIST:

- **Q.** What is need of Design for Testability (DFT) in VLSI IC design and explain Built in Self Test (BIST) techniques of DFT. **(WINTER 2023, 7 Marks; SUMMER 2024, 7 Marks OR; SUMMER 2025, 3 Marks OR; SUMMER 2026, 7 Marks OR)**

Other Important Questions:

1. DFT Techniques (Theory):

- **Q.** How partition and Mux technique is used to increase the testability of circuits? **(WINTER 2022, 3 Marks OR)**
- **Q.** Explain scan-based techniques for DFT with one example. **(WINTER 2025, 4 Marks OR)**

Chapter 11: FinFET Device

Repeated Questions:

1. FinFET:

- **Q.** Compare FinFET and Planar MOSFET. **(SUMMER 2022, 3 Marks OR; SUMMER 2024, 3 Marks; WINTER 2024, 3 Marks OR; SUMMER 2025, 7 Marks OR; WINTER 2025, 3 Marks OR; SUMMER 2026, 3 Marks - includes advantages and disadvantages)**
- **Q.** Draw diagram of FinFET and discuss its structure/advantages. **(WINTER 2022, 4 Marks OR; WINTER 2023, 3 Marks)**

Other Important Questions:

None identified.

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