Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE – SEMESTER- V EXAMINATION-SUMMER 2023

Subject Code: 3151107 Date: 26/06/2023

Subject Name: Advance Microcontroller

Time: 02:30 PM TO 05:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Compare RISC and CISC philosophy.	**03**
	(b)	List the features rejected from RISC Design for improved ARM Design.	**04**
	(c)	Draw and explain ARM Core data flow model.	**07**
Q.2	**(a)**	Describe the load store architecture used in ARM controller.	**03**
	(b)	Explain the ARM7TDMI programmer's model.	**04**
	(c)	Explain following ARM instruction with example: 1)UMULL 2)SBCS 3)BL 4)BIC 5)RSC 6)EORS 7)MOVEQ	**07**
		OR	
	(c)	Write a program to count a number of 1's in R0. Assume that R0 contains any 32-bit data.	**07**
Q.3	**(a)**	Describe software interrupt instruction SWI with its importance.	**03**
	(b)	Explain barrel shifter instructions with example.	**04**
	(c)	Explain the 5-stage Pipeline architecture used in ARM controller with necessary figures.	**07**
		OR	
Q.3	**(a)**	Explain the BX instruction with suitable example.	**03**
	(b)	Explain how register allocated by ARM C compiler.	**04**
	(c)	Write a short note on stack implementation in ARM.	**07**
Q.4	**(a)**	List the portability issues encounter when porting C code to the ARM.	**03**
	(b)	Draw and explain the memory hierarchy used in a computer system.	**04**
	(c)	Write a C program to blink LED connected to pin P0.3 at the interval of 1 second in LPC2148. Generate a delay using Timer.	**07**
		OR	
Q.4	**(a)**	Explain control flow instructions for ARM controller with suitable examples.	**03**
	(b)	Briefly discuss the Thumb Programmers model.	**04**
	(c)	Explain ARM addressing modes with suitable examples.	**07**
Q.5	**(a)**	Write down the MMU Advantages for ARM processor.	**03**
	(b)	Explain mapping a task in virtual memory to physical memory using a relocation register.	**04**
	(c)	Discuss the APB bus transfers. Explain the need of APB bridge.	**07**
		OR	
Q.5	**(a)**	Briefly discuss the AHB bus features.	**03**
	(b)	Explain the unified split cache memory.	**04**
	(c)	Discuss Tightly coupled Memory (TCM).	**07**

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