Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–V (NEW) EXAMINATION – WINTER 2023

Subject Code:3151105 Date:13-12-2023

Subject Name:VLSI Design

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**
5. **Note: Use following parameters for computation if required.**
   Boltzmann constant = 1.38×10^{-23} (J/K), q = 1.6×10^{-19} C, $n_i = 1.45 \times 10^{10}$ cm^{-3}, $\varepsilon_{Si} = 11.7\varepsilon_0$, $\varepsilon_0 = 8.85\times10^{-14}$ F/cm , $\varepsilon_{ox} = 3.97\varepsilon_0$ F/cm

			Marks
Q.1	**(a)**	Identify following statements are True or False. Make correction if false and justify. (i) NMOS is constructed on n type and PMOS is constructed on p type substrate. (ii) If substrate is connected with V_{DD} then threshold voltage $V_T = V_{T0}$ (iii) If V_{DS} is constant and V_{GS} increases then current I_{DS} in NMOS transistor will increase.	**03**
	(b)	For MOS structure, derive the expression for the maximum possible depth of the depletion region.	**04**
	(c)	Draw cross section of n-channel MOSFET. Obtain drain current expression as a function of V_{GS}, V_{DS}, and V_{BS} for linear and saturation region of operation of MOSFET device.	**07**
Q.2	**(a)**	Answer the following questions. (i) Which material is used for gate formation of CMOS transistor? (ii) What is feature size? (iii) Among BJT and MOS which device is smaller in size?	**03**
	(b)	Describe usage of photo resist in lithography process.	**04**
	(c)	Explain two types of scaling with its advantages and disadvantages.	**07**
		OR	
	(c)	Draw circuit of resistive load inverter. Derive expression for V_{IH}, V_{IL}, V_{OL} and V_{OH} for resistive load inverter.	**07**
Q.3	**(a)**	Consider a p-channel MOSFET with parameters μ_p = 300 cm^2/V-s, $C_{ox} = 6.9 \times 10^{-8}$ F/cm^2, (W/L) = 10, and V_{TP} = -0.65V. Determine the maximum current at V_{GS} = -3V.	**03**
	(b)	Derive expression of threshold voltage for CMOS inverter.	**04**
	(c)	Consider reverse biased abrupt silicon p-n junction. The doping density of the n-type region is $N_D = 10^{19}$ cm^{-3} and the doping density of the p-type region is given as $N_A = 10^{16}$ cm^{-3}. The junction area is A = 20µm x 20µm. Calculate the built-in junction potential and zero bias junction capacitance per unit area for the structure.	**07**
		OR	
Q.3	**(a)**	Discuss methods to estimate interconnect parasitic.	**03**
	(b)	Explain switching power dissipation of CMOS inverter.	**04**

	(c)	Calculate the threshold voltage V_{TO} and substrate bias coefficient at $V_{SB}=0$, for silicon gate n-channel MOS transistor, with the following parameters: substrate doping density $N_A=3\times10^{16}$ cm-3, $N_D = 4\times10^{19}$ cm-3, gate oxide thickness tox = 200A°, and oxide interface fixed charge density Nox = 10^{10} cm^{-2}. Assume $\phi_{F(gate)}$ = 0.56V.	**07**
Q.4	**(a)**	Draw diagram of FinFET and discuss its advantages.	**03**
	(b)	Draw diagram of ring oscillator. For five stage ring oscillator circuit, derive expression for frequency of oscillation.	**04**
	(c)	What is need of design for testability? Explain Adhoc testable design techniques and built-in SelfTest (BIST) techniques.	**07**
		OR	
Q.4	**(a)**	List packaging technology used for VLSI chips.	**03**
	(b)	Draw the optimized stick diagram for the following function (CMOS logic) using Euler path approach, $X = \overline{ADF + B(E + C)}$	**04**
	(c)	Draw CMOS negative edge triggered master slave D flip flop and explain its working with proper circuit diagram.	**07**
Q.5	**(a)**	List examples of physical defects during chip fabrication.	**03**
	(b)	Draw 2 input NAND gate using complementary pass transistor logic.	**04**
	(c)	What is importance of CMOS Transmission gate? Draw 2×1 MUX using compound gate and compare it with 2×1 MUX based on transmission gate. Also draw 4×1 MUX based on transmission gate.	**07**
		OR	
Q.5	**(a)**	Realize XOR gate using CMOS transmission gate.	**03**
	(b)	Explain the need of Voltage bootstrapping? Derive the mathematical expression for dynamic Voltage bootstrapping circuit.	**04**
	(c)	Draw and explain 'Y' chart for the VLSI design flow.	**07**

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