Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–V (NEW) EXAMINATION – WINTER 2022

Subject Code:3151105 Date:13-01-2023

Subject Name:VLSI Design

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

Q.1	**(a)**	What is reliability of the chip? List the 4 major causes for chip reliability problems.	**03**
	(b)	Explain the impact of full-custom and semi-custom VLSI design style on design cycle time and circuit performance.	**04**
	(c)	Explain the process steps for fabrication of n-type MOSFET.	**07**
Q.2	**(a)**	Draw the VTC of resistive load inverter circuit and show the 3 different operating regions of MOSFET of the circuit on it.	**03**
	(b)	What is channel length modulation effect?	**04**
	(c)	Explain the MOS system under external bias for accumulation and inversion region.	**07**
		OR	
	(c)	Derive the drain current I_D equation for n-type MOSFET using gradual channel approximation.	**07**
Q.3	**(a)**	Elaborate different clock distribution network.	**03**
	(b)	Draw and explain the operation of two input multiplexer using CMOS transmission gates.	**04**
	(c)	Derive the equation of V_{IL} and V_{IH} for CMOS inverter.	**07**
		OR	
Q.3	**(a)**	What is Latch-up in CMOS chip?	**03**
	(b)	For the function Z = $\overline{A(D+E)+BC}$. Construct dual pull up graph from pull down graph using Dual Graph Concept.	**04**
	(c)	Consider a CMOS Inverter circuit with the following parameters: V_{DD}= 3.3V, $V_{TO,n}$ = 0.6V, $V_{TO,p}$ = - 0.7V, k_n = 400 μA/V^2, k_p =160 μA/V^2 . Find the value of V_{IL}.	**07**
Q.4	**(a)**	Explain constant field scaling for MOSFET.	**03**
	(b)	Illustrate the RC delay models for calculation of interconnect delay.	**04**
	(c)	Derive the equation for propagation delay of output signal during high to low transition of output of CMOS inverter circuit with C_{load} as load capacitance.	**07**
		OR	
Q.4	**(a)**	Draw the circuit of dynamic D-latch.	**03**
	(b)	What are controllability and observability? Discuss in brief.	**04**
	(c)	Explain the working of clocked NOR based SR latch with gate level circuit and waveform. Draw the AOI based implementation of this circuit.	**07**
Q.5	**(a)**	What are the advantages of FinFET over planner MOSFET?	**03**
	(b)	What is substrate bias effect? For two input depletion load NAND gate, how many MOSFET have this effect?	**04**

	(c)	How pre-charge and evaluate logic works for dynamic CMOS circuit? Explain with example.	**07**

OR

Q.5	**(a)**	How partition and Mux technique is used to increase the testability of circuits?	**03**
	(b)	Draw and explain the basic structure of FinFET device.	**04**
	(c)	Explain NORA CMOS logic and its advantages.	**07**

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