Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–V EXAMINATION – SUMMER 2025

Subject Code:3151105 Date:20-05-2025

Subject Name:VLSI Design

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Present device isolation techniques in fabrication process.	**03**
	(b)	Explain the MOS system under external bias.	**04**
	(c)	Describe the working of edge-triggered flip-flops with necessary diagrams.	**07**
Q.2	**(a)**	Explain the basic principles of pass transistor circuits.	**03**
	(b)	Design 2-input OR, AND and XOR gate using CMOS.	**04**
	(c)	Present the analysis of the resistive load inverter. Derive critical voltages and noise margins.	**07**
		OR	
	(c)	Analyze transmission gates (TGs) in detail. Also, describe the procedure for circuit design with TGs.	**07**
Q.3	**(a)**	Enlist MOSFET scaling and small-geometry effects.	**03**
	(b)	Discuss synchronous dynamic circuit techniques.	**04**
	(c)	Present timing analysis of CMOS inverter.	**07**
		OR	
Q.3	**(a)**	What is the built-in self-test (BIST)? Explain this technique in brief.	**03**
	(b)	Describe the behavior of bistable elements.	**04**
	(c)	Explain voltage bootstrapping.	**07**
Q.4	**(a)**	Write the equations describing the current-voltage characteristics of MOSFET.	**03**
	(b)	Describe fabrication of nMOS Transistor.	**04**
	(c)	Analyze the factors behind latch-up problems. Also, explain the techniques for its prevention.	**07**
		OR	
Q.4	**(a)**	What is the substrate bias effect? Explain its analysis.	**03**
	(b)	Discuss switching power dissipation of CMOS inverters.	**04**
	(c)	Present the analysis of on-chip clock generation and distribution techniques.	**07**
Q.5	**(a)**	Define and explain DIBL.	**03**
	(b)	Present delay-time definitions.	**04**
	(c)	Discuss fault types and models.	**07**
		OR	
Q.5	**(a)**	Explain controllability and observability.	**03**
	(b)	Describe the operating principle of the SR latch circuit with the necessary diagrams.	**04**
	(c)	What are the needs of FinFET devices? Explain FinFET devices in detail. Also, compare them with planar MOSFET.	**07**

****