Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–V (NEW) EXAMINATION – SUMMER 2024

Subject Code:3151105 Date:23-05-2024

Subject Name:VLSI Design

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Compare semicustom and Full custom VLSI design style.	**03**
	(b)	Discuss following approaches used to reduce complexity of IC design i) Hierarchy ii) Regularity iii) Modularity iv) Locality	**04**
	(c)	Draw and explain various fabrication steps for CMOS inverter with proper notations at each fabrication steps.	**07**
Q.2	**(a)**	Explain MOSFET capacitance in brief.	**03**
	(b)	Derive the drain current equation for MOSFET using Gradual Channel Approximation (GCA)	**04**
	(c)	Find the depletion layer width, depletion region charge and threshold voltage with no substrate bias with the following physical parameters. Physical parameters VSB=0, for silicon gate n channel MOS transistor, with the following parameters: Substrate doping density NA=1.5 x 10^{16} cm^{-3}, Gate donor doping N_D = 10^{18} cm^{-3}, Gate oxide thickness tox = 400A°, Nss = 10 x 10^{10} cm^{-3}. Consider Boltzmann Constant = 1.38 x10^{-23} (J/K), Electron charge = 1.6 x 10^{-19} C, Intrinsic Silicon carrier concentration ni= 1.45 x 10^{10} cm^{-3}, ε_Si = 1.035 x 10^{-12} F/cm ε_0 = 8.85x10^{-14} F/cm, εox = 0.345 x 10^{-12} F/cm.	**07**
		OR	
	(c)	For an enhancement type NMOS transistor has its source terminal connected to ground and 3 V connected to ground and 3 V connected to the gate. NMOS has V_T= 2 V , λ= 0.04 1/V , μ_n *C_{ox}=20A/V^2, W= 200μm and L =10μm , V_G= 3V , V_D=0.5 V and 1 V. Calculate Drain Current I_D. **Physical constants** : Thermal voltage =KT/q = 0.026 volt. Energy Gap of silicon (Si) =E_g = 1.12 Ev. Intrinsic Carrier Concentration of silicon=n_i=1.45x$10^{10}$$cm^{-3}$. Dielectric constant of vaccume =ε_o=8.85 x 10-^{14}F/cm. Dielectric constant of silicon =ε_{si}= 11.7 xε_oF/cm. Dielectric constant of silicon dioxide =ε_{ox}= 3.97 xε_oF/cm	**07**
Q.3	**(a)**	What is meant by static and dynamic power dissipation?	**03**

(b) Define propagation delay and derive the expression for τpHL for CMOS inverter. Assume ideal step as an input to CMOS inveter. **04**

(c) Consider a resistive load inverter circuit with V_{DD}=5 V, Kn' =10μA/V^2 V_{TO}=0.8V,RL=400kΩ and W/L=2.Calculate the critical Voltages (V_{OH},V_{OL},V_{IL} and V_{IH}) on the VTC and find the noise margins of the circuit. **07**

OR

Q.3 **(a)** Draw CMOS inveter. Explain its voltage transfer characteristic. Also explain the NML and NMH noise margins with respect to this transfer characteristic **03**

4.4.13

(b) Draw the inverter circuit with depletion type nMOS load. Mention the operating regions of driver and load transistors for different input voltages. Derive critical voltage points V_{OH}, V_{OL} , V_{IH} and V_{IL} for depletion- load nMOS inverter **04**

(c) Consider a CMOS inverter with the following parameters: **07**
VDD=3.3 V, $VT0,n$= 0.6 V, $VT0,p$= −0.7 V ,kn= 200 $\mu A/V^2$ and kp= 160 $\mu A/V^2$
Calculate the noise margins of the circuit. Consider k_R=2.5 V and $V_{T0,n} \neq |V_{T0,p}|$ as it is not a symmetric CMOS inverter.

Q.4 **(a)** What are the limitations of Dynamic circuits? Discuss the effect of charge sharing and charge leakage in dynamic pass transistor logic. **03**

(b) Two nMOS transistors (M1 and M2) connected in series is shown in Figure 1. The power supply is VDD =3.3 V and the nMOS threshold V_{TN} = 0.55 V. Find the output voltage at node b. Consider i) Va = 2.7 V and ii) Va = 3V. **04**

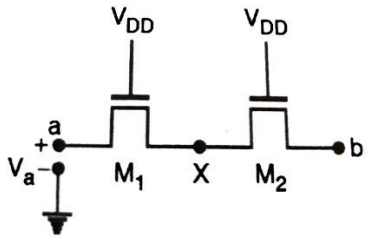

Figure 1

(c) Explain the Euler path approach to find the optimized stick-diagram for any CMOS logic circuit. Draw the optimized stick-diagram for the following Boolean function (CMOS Logic), F= (A(D+E)+ BC)'. Explain the importance of Euler path approach. **07**

OR

Q.4 **(a)** What do you mean by stick diagram? Implement the following Boolean function using stick diagram. **03**
Y = (A*(D+E)+B*C)'

(b) Explain the need of Voltage bootstrapping? Derive the mathematical expression for dynamic Voltage bootstrapping circuit. **04**

(c) For the Exclusive OR function , draw with following realization **07**
1. Static CMOS realization
2. Pseudo nMOS gate
3. CMOS Transmission Gate(TG)

Q.5 **(a)** Compare FinFET and Planner MOSFET **03**

(b) Draw transistor level circuit diagram of NAND based SR latch using CMOS. **04**

	(c)	What is clock-skew? Explain on-chip clock generation and distribution.	**07**
		OR	
Q.5	**(a)**	Draw and discuss three stage ring oscillator	**03**
	(b)	Implement and Describe CMOS clocked SR flip-flop	**04**
	(c)	What is need of Design of Testability (DFT) in VLSI IC design and explain Built in Self Test (BIST) techniques of DFT	**07**

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