Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE – SEMESTER- V EXAMINATION-SUMMER 2023

Subject Code: 3151105 Date: 28/06/2023

Subject Name: VLSI Design

Time: 02:30 PM TO 05:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

Q.1	**(a)**	What is the role of photo resist material in IC fabrication process?	**03**
	(b)	Describe concepts of Regularity and Modularity.	**04**
	(c)	What is the impact of different VSLI Design styles upon the design cycle time and achievable circuit performance?	**07**
Q.2	**(a)**	Compare constant voltage scaling and constant field scaling.	**03**
	(b)	Note down physical parameters affecting the threshold voltage of MOS structure.	**04**
	(c)	Write down basic steps of Local oxidation of Silicon (LOCOS) process.	**07**
		OR	
	(c)	What is channel length modulation? How it affects drain current of MOSFET?	**07**
Q.3	**(a)**	Define: Propagation delay, Rise time and Fall time.	**03**
	(b)	What is hot carrier effect and punch through in small geometries devices?	**04**
	(c)	Explain the junction capacitances associated with MOS structure.	**07**
		OR	
Q.3	**(a)**	Discuss 3 stage CMOS ring oscillator circuit with necessary waveforms.	**03**
	(b)	Explain: Body effect and Noise margin.	**04**
	(c)	Give the comparison of resistive load, depletion load and CMOS inverter circuits.	**07**
Q.4	**(a)**	Draw transmission gate implementation of XOR gate.	**03**
	(b)	Show with the diagram, bias conditions and operating regions of CMOS transmission gate, as a function of output voltage.	**04**
	(c)	In CMOS inverter circuit, define propagation delay τ_{PLH} (low-to-high transition at output) and obtain its expression.	**07**
		OR	
Q.4	**(a)**	Draw CMOS implementation of D latch.	**03**
	(b)	Explain basic principles of Pass transistor circuits.	**04**
	(c)	Draw CMOS circuit for NAND gate and derive threshold voltage equation for it.	**07**
Q.5	**(a)**	Explain cascading problem in dynamic CMOS logic.	**03**
	(b)	Draw and explain the basic circuit architecture of Zipper CMOS circuits with clock signals.	**04**
	(c)	Differentiate the ratioed and ratio less dynamic logic circuits with examples.	**07**
		OR	
Q.5	**(a)**	Give examples of physical defects.	**03**
	(b)	Explain controllability and Observability.	**04**
	(c)	What is latch up in CMOS circuits and how it can be prevented?	**07**