Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–V(NEW) EXAMINATION – SUMMER 2022

Subject Code:3151105 Date:13/06/2022

Subject Name:VLSI Design

Time:02:30 PM TO 05:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Define concept of : Modularity, Locality and Regularity	**03**
	(b)	Explain accumulation, depletion and inversion of MOS under external bias.	**04**
	(c)	Explain process flow of fabrication of nMOS transistoron p-type silicon.	**07**
Q.2	**(a)**	Explain in short: FPGA	**03**
	(b)	What is transmission gate?	**04**
	(c)	Derive MOSFET current -voltage characteristics using gradual channel approximation.	**07**
		OR	
	(c)	Measured voltage and current data for a MOSFET are given below: Determine the type of the device and calculate the parameters k_n, V_{TO}, and γ. Assume φ_F = -0.3V. Assume MOSFET is enhancement type and neglect channel length modulation effect.	**07**

V_{GS}**(V)**	V_{DS}(V)	V_{SB}(V)	I_D (μa)
3	3	0	97
4	4	0	235
5	5	0	433
3	3	3	59
4	4	3	173
5	5	3	347

Q.3	**(a)**	Explain noise margin.	**03**
	(b)	Explain rise time and fall time of inverter using diagram.	**04**
	(c)	Consider a resistive load inverter circuit with V_{DD}= 5V, k_n' =20μA/V^2, V_{TO} = 0.8V, R_L = 200kΩ and W/L =2. Calculate critical voltages (V_{OL}, V_{OH}, V_{IL}, V_{IH}) and find the noise margins of the circuit.	**07**
		OR	
Q.3	**(a)**	Explain voltage transfer characteristics of inverter.	**03**
	(b)	Explain propagation delay time for inverter: τ_{PLH}, τ_{PHL}	**04**
	(c)	Explain CMOS inverter and find equation of V_{IL} and V_{IH}.	**07**
Q.4	**(a)**	Explain different fault types in chip.	**03**
	(b)	Explain two input CMOS NOR gate.	**04**
	(c)	Explain Elmore delay with suitable diagram.	**07**
		OR	
Q.4	**(a)**	What is latch-up? Write causes of latch- up.	**03**

	(b)	Draw CMOS implementation of XOR function.	**04**
	(c)	Explain CMOS ring oscillator circuit.	**07**
Q.5	**(a)**	Explain Controllability and Observability.	**03**
	(b)	Design CMOS SR latch circuit based on NOR gate.	**04**
	(c)	Explain Domino CMOS logic.	**07**

OR

Q.5	**(a)**	Compare FinFET and Planner MOSFET.	**03**
	(b)	Explain CMOS implementation of D - latch.	**04**
	(c)	Explain voltage bootstrapping.	**07**

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