Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER–VII (NEW) EXAMINATION – WINTER 2024

Subject Code:3171111 Date:19-11-2024

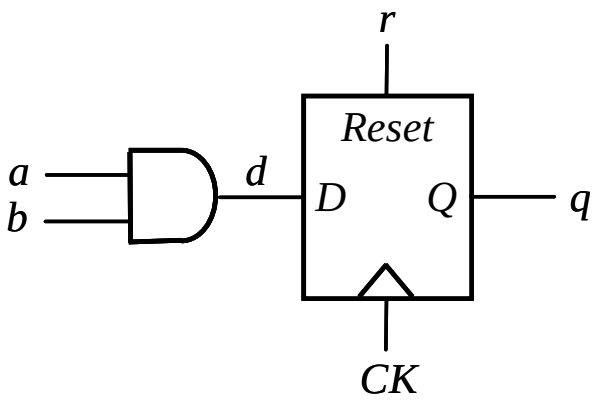
Subject Name: Testing and Verification

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

Q.1	**(a)**	Draw flow chart of VLSI development process with mentioning involved testing at each stage.	**03**
	(b)	Define following terms respect to VLSI testing: 1. Yield, 2. Reject rate, 3. Fault coverage and 4. Fault detection efficiency.	**04**
	(c)	Draw two - inputs CMOS NOR gate and write truth table for fault-free circuit and all possible transistor faults. Discuss how to detect all possible transistor faults in this circuit and define and calculate collapse faults.	**07**
Q.2	**(a)**	What is goal of design for testability (DFT) and enlist three basic approaches of DFT.	**03**
	(b)	Define Controllability, observability, testability and testability analysis. Enlist testability analysis techniques.	**04**
	(c)	Write SCOAP combination controllability and observability calculation rules of different logic gates. Find combinational controllability and observability of Half Adder logic circuit at different site using SCOAP analysis techniques.	**07**
		OR	
	(c)	Derive equation of combinational and sequential controllability and observability of a, b, d, r, CK and q sites for given circuit using SCOAP techniques.	**07**



Q.3	**(a)**	Compare Muxed D, Clocked and LSSD scan cells.	**03**
	(b)	What is scan design rule of derived clock based design and explain it recommended solution with an example.	**04**
	(c)	Enlist three different scan design architecture of DFT. Explain Muxed-D based full scan design architecture in detail.	**07**

OR

Q.3	**(a)**	Draw a flow chart of logic simulation for digital circuit design verification.	**03**
	(b)	Write truth table of four valued logic (0, 1, u, z) 2- inputs AND and OR gates and compare binary logic with four valued logic.	**04**
	(c)	Enlist various algorithms for fault simulation and explain serial fault simulation in detail with algorithm flow chart and example.	**07**
Q.4	**(a)**	Define Transport and Inertial Delay with an example.	**03**
	(b)	Enlist different stages of compile code simulation with its function and draw flow chart of logic levelization.	**04**
	(c)	Define controlling and inversion values of different logic gates (AND, OR, NAND and NOR). Explain input scanning algorithm with flow chart.	**07**

OR

Q.4	**(a)**	What are the advantages of design and verification reuse.	**03**
	(b)	What is test bench? Differentiate: Testing and Verification	**04**
	(c)	What is linting tool? Explain linting verilog source code and limitation of linting tools.	**07**
Q.5	**(a)**	What is assertion? What are the two broad classes of assertion	**03**
	(b)	What are the different approaches of functional verification? Elaborate any one approach.	**04**
	(c)	What is code coverage? And explain it in details. What does 100% code coverage mean?	**07**

OR

Q.5	**(a)**	Enlist purposes of matric as verification tool.	**03**
	(b)	What do you mean by verification intellectual property?	**04**
	(c)	Design 4x1 multiplexer logic design using VHDL/Verilog HDL and write it test bench.	**07**

****