Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VII (NEW) EXAMINATION – WINTER 2023

Subject Code:3171111 Date:01-12-2023

Subject Name:Testing and Verification

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Write down importance of VLSI Testing.	**03**
	(b)	What are the challenges in VLSI Testing?	**04**
	(c)	Define following: 1. Yield 2. Reject Rate 3. Reliability 4. Fault 5. Failure 6. Error 7. Repair time	**07**
Q.2	**(a)**	Write down the controlling value and inversion value for the different logic gates.	**03**
	(b)	What is fault collapsing? How it is useful in testing?	**04**
	(c)	What is bridging fault? Explain various bridging fault models.	**07**
		OR	
	(c)	Explain Muxed-D full scan design architecture in detail.	**07**
Q.3	**(a)**	Write down names of typical ad hoc DFT techniques.	**03**
	(b)	Find out SCOAP and Probability based testability measures for 5 input NAND gate.	**04**
	(c)	Explain Control point insertion.	**07**
		OR	
Q.3	**(a)**	What is combinational feedback loop? How it is avoided in scan design?	**03**
	(b)	Explain Clocked scan cell with necessary waveform.	**04**
	(c)	Why is it difficult to test sequential circuit? How scan design concept will help to solve the problem of testing sequential circuit?	**07**
Q.4	**(a)**	Write down main decisions that are made at scan configuration stage in scan design flow.	**03**
	(b)	Compare: Fault simulation and Logic simulation	**04**
	(c)	Explain parallel gate evaluation with the help of an example.	**07**
		OR	
Q.4	**(a)**	Explain Inertial delay.	**03**
	(b)	What is meant by verification plan? Discuss its importance in verification.	**04**
	(c)	What is Compiled Code Simulation? Draw and Explain Compiled Code Simulation flow.	**07**
Q.5	**(a)**	Compare: Testing and Verification	**03**
	(b)	Explain: Grey box verification and White box verification	**04**
	(c)	Design 4x1 multiplexer and write its testbench in any hardware description language (HDL)	**07**
		OR	
Q.5	**(a)**	What is reconvergence model in verification?	**03**
	(b)	Write down different approaches of functional verification and define all.	**04**
	(c)	What is the role of code coverage in verification? Explain it in detail.	**07**