Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VII (NEW) EXAMINATION – WINTER 2022

Subject Code:3171111 Date:16-01-2023

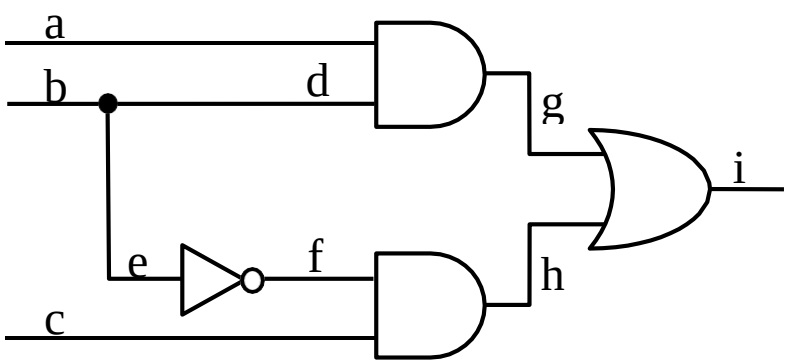
Subject Name:Testing and Verification

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Differentiate following terms: Testing and Verification	**03**
	(b)	Define following: 1. Yield, 2. Reject rate, 3. Online testing, 4. Fault detection efficiency.	**04**
	(c)	Consider the combinational logic circuit in Figure. How many possible single stuck-at faults does this circuit have? How many collapsed single stuck at faults does this circuit have? Determine input test vectors that can detect all single stuck-at fault.	**07**



Q.2	**(a)**	Define mean time between failure, mean time to repair and system availability.	**03**
	(b)	What is Fault modelling and its requirement? List different fault models.	**04**
	(c)	Discuss all the possible transistor faults in two-input CMOS NOR gate and the method of testing each of them.	**07**
		OR	
	(c)	Explain all possible bridging fault models with circuit diagram and truth table.	**07**
Q.3	**(a)**	What is need of DFT techniques and Define following terms: (i) Controllability (ii) Observability	**03**
	(b)	What do you mean by testability? Also explain the meaning of testability analysis.	**04**
	(c)	Write SCOAP combination controllability and observability calculation rule of different logic gates. Find combination controllability and observability of 1 bit full adder using SCOAP technique.	**07**
		OR	
Q.3	**(a)**	Compare Muxed D , Cloked and LSSD scan cells	**03**
	(b)	Write probability based controllability and observability calculation rules of different logic gates.	**04**
	(c)	Draw and explain scan design flow.	**07**

Q.4	**(a)**	Enlist various algorithms for fault simulation	**03**
	(b)	Discuss the Transport Delay, Inertial Delay, wire delay and functional element delay in brief.	**04**
	(c)	Explain serial fault simulation algorithm with an example.	**07**
		OR	
Q.4	**(a)**	What is reconvergence model in verification?	**03**
	(b)	What is Linting tools and its limitations?	**04**
	(c)	What are the different function verification approaches and explain each in details with its advantages and disadvantages.	**07**
Q.5	**(a)**	What is assertion and its importance in verification?	**03**
	(b)	What is importance and role of verification plan?	**04**
	(c)	Draw and explain Enhanced Scan Architecture.	**07**
		OR	
Q.5	**(a)**	Draw flow chart of logic simulation for design verification.	**03**
	(b)	Explain scan design rule for Derived clock design style and give recommended solution	**04**
	(c)	Explain compile code simulation techniques in detail.	**07**

****