Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VII EXAMINATION – SUMMER 2025

Subject Code:3171111 Date:08-05-2025

Subject Name:Testing and Verification

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

Q.1	**(a)**	Write down challenges in VLSI Testing.	**03**
	(b)	Compare: Testing and Verification.	**04**
	(c)	Define following terms: 1. Equivalent Faults 2. Fault 3. Reject Rate 4. Rule of Ten 5.Fault coverage 6. Defect level 7. Fault detection efficiency	**07**
Q.2	**(a)**	Explain bridging fault models.	**03**
	(b)	Obtain Controllability and Observability for various signals of 5 inputs OR Gate using SCOAP and Probability based testability analysis.	**04**
	(c)	Explain testing methodology for transistor faults in two-input CMOS NAND Gate.	**07**
		OR	
	(c)	What is mean by scan design rules? Explain scan design rules for following design styles. 1.Derived Clocks 2.Combinational feedback loops	**07**
Q.3	**(a)**	Calculate number of collapsed faults for two inputs CMOS NOR Gate.	**03**
	(b)	Explain input scanning method for logic element evaluation.	**04**
	(c)	Draw and explain Clocked scan cell design with the help necessary waveforms.	**07**
		OR	
Q.3	**(a)**	What are the advantages of parallel fault simulation? Name the different approaches of it.	**03**
	(b)	Explain toggle coverage and fault sampling.	**04**
	(c)	Draw and explain scan design flow.	**07**
Q.4	**(a)**	Explain logic optimization process for logic simulation.	**03**
	(b)	Draw and explain two pass for nominal event driven strategy.	**04**
	(c)	What is the need of timing models in testing? List down various time models and explain any one of them in detail.	**07**
		OR	
Q.4	**(a)**	What is the importance and role of verification plan?	**03**
	(b)	Write a VHDL/Verilog code and test bench for 1 X 4 demux.	**04**
	(c)	Draw and explain flowchart indicating steps to do concurrent fault simulation.	**07**
Q.5	**(a)**	What is mean by functional coverage? How it is useful in verification flow?	**03**
	(b)	What is code coverage? Explain its role in verification.	**04**
	(c)	Compare following: White box verification, Black box verification and Grey box verification.	**07**
		OR	
Q.5	**(a)**	Differentiate between static hazard and dynamic hazard.	**03**
	(b)	Compare Code driven simulation and event driven simulation	**04**
	(c)	Draw and explain verification flow.	**07**

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