Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE – SEMESTER- VII EXAMINATION-SUMMER 2023

Subject Code: 3171111 Date: 21/06/2023

Subject Name: Testing and Verification

Time: 10:30 AM TO 01:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

Q.1	**(a)**	Calculate number of collapsed faults for two input CMOS NAND Gate.	**03**
	(b)	Define following: 1. Rule of Ten 2. Equivalent faults 3. Fault collapsing 4. Fault	**04**
	(c)	What is bridging fault? Explain various bridging fault models.	**07**
Q.2	**(a)**	List down the challenges in VLSI testing.	**03**
	(b)	Define following :1. Delay fault 2. Pattern sensitivity fault 3. Coupling fault 4. Exhaustive testing	**04**
	(c)	Explain testing methodology for transistor faults in two-input CMOS NOR Gate.	**07**
		OR	
	(c)	Discuss logic levelization algorithm with the help of an example.	**07**
Q.3	**(a)**	Explain scan stitching.	**03**
	(b)	What is mean by scan design rules? Explain scan design rules for combinational feedback loops.	**04**
	(c)	What is Hazard? Explain various types of hazards.	**07**
		OR	
Q.3	**(a)**	List and explain different level of abstraction in VLSI testing.	**03**
	(b)	Discuss scan configuration and its importance in scan design flow.	**04**
	(c)	Explain deductive fault simulation.	**07**
Q.4	**(a)**	Write down the truth table of AND, OR and NOT gate using ternary logic.	**03**
	(b)	Calculate probability-based measures for 3 input OR gate.	**04**
	(c)	Draw and explain LSSD scan cell design with the help necessary waveforms.	**07**
		OR	
Q.4	**(a)**	List out different ad-hoc testing technique for VLSI design.	**03**
	(b)	Compare: Testing and Verification	**04**
	(c)	Explain input scanning algorithm.	**07**
Q.5	**(a)**	Explain equivalence checking.	**03**
	(b)	System Verilog is preferred over other hardware verification languages to implement Test benches in industry. Why?	**04**
	(c)	Explain different functional verification approaches.	**07**
		OR	
Q.5	**(a)**	Discuss role of verification plan.	**03**
	(b)	What is code coverage? What does 100% code coverage mean?	**04**
	(c)	Design half adder and write it test bench using any hardware description language.	**07**