Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VII (NEW) EXAMINATION – SUMMER 2022

Subject Code:3171111 Date:14/06/2022

Subject Name:Testing and Verification

Time:02:30 PM TO 05:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

Q.1	**(a)**	What is the importance of Testing in VLSI Design Flow?	**03**
	(b)	Define yield and reject rate for VLSI Testing and discuss its importance in VLSI Testing.	**04**
	(c)	Explain the **Defect**, **Fault** and **Error** terms used in VLSI Testing with the help of an example.	**07**
Q.2	**(a)**	Compare: online testing and offline testing.	**03**
	(b)	Which are the different delay fault models used in VLSI Testing? Explain any one of them.	**04**
	(c)	Explain testing methodology for transistor faults in two-input CMOS NAND Gate.	**07**
		OR	
	(c)	Which model is used to model open and short faults in wires that interconnect the transistors in VLSI circuits? Explain it in details.	**07**
Q.3	**(a)**	What are the advantages of parallel fault simulation? Name the different approaches of it	**03**
	(b)	What is mean by scan design rules? Explain scan design rules for Gated Clocks.	**04**
	(c)	Give comparison of fault simulation techniques.	**07**
		OR	
Q.3	**(a)**	Write down the names of different special purpose scan designs used in VLSI Design.	**03**
	(b)	Compare compiled code simulation and event driven simulation.	**04**
	(c)	Explain differential fault simulation.	**07**
Q.4	**(a)**	How the signaling will be provided in scan chain in which a negative edge scan cell is followed by a positive scan cell?	**03**
	(b)	Draw and explain clocked scan cell design with the help necessary waveforms.	**04**
	(c)	Calculate SCOAP and Probability based testability measures for a 3 input NOR gate.	**07**
		OR	
Q.4	**(a)**	What do you mean by testability? Also explain the meaning of testability analysis.	**03**
	(b)	Write down importance of assertions in verification.	**04**
	(c)	Explain any one structured approach of Design for testability.	**07**
Q.5	**(a)**	Compare White box verification and Black box verification.	**03**
	(b)	What are the limitations of linting tools?	**04**
	(c)	Explain different types of code coverages.	**07**
		OR	
Q.5	**(a)**	Explain verification flow.	**03**
	(b)	What is the importance and role of verification plan?	**04**
	(c)	Design 1x4 demultiplexer and write it test bench using any hardware description language.	**07**